Integrated Inductor Actively Engaging Metal Filling Rules

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***Abstract*— This paper reports a new strip-patterned integrated inductor that actively engages metal filling rules leading to reduced manufacturing cost and process-induced uncertainties while simultaneously maintaining state-of-the-art performance. The strip-patterned inductor consists of parallel horse shoe-shape metal lines in the foot print of a single-line inductor. It observes back-end-of-line (BEOL) metal density rules by design, and it is not subject to a post-layout patterning to enforce metal density on a large piece of metal. As a result, better model-to-hardware correlation (MHC) is expected. The new inductor structure is backed by experimental and simulated results that demonstrate the design methodology in the presence of process uncertainties typically not known to the circuit designer.**

I. Introduction

High-quality (Q) on-chip inductor integration is essential for RF system-on-chip manufacturing [1-3]. The integration of on-chip inductor enables multiple communication systems implemented on high-performance digital processors. This is especially critical when the input and output channel capacities become the bottleneck in intensive computations. In nanometer technologies on-chip high-performance inductors face an additional challenge, namely efficient manufacturing [4-7]. Efficient manufacturing depends primarily on the physical structure repeatability, parasitic metals, mask processing time, and model-to-hardware correlation. For example, state-of-the-art technologies with more than ten metal layers need to meet minimum and maximum metal filling ratio rules for each layer. These rules are often imposed by chemical and mechanical polishing (CMP) process used to maintain planarity of each metal layer. While these metal filling rules are important for high-yield manufacturing, they often prove particularly challenging for high-Q inductors. Typically high-Q and high-power handling inductors require long-and-wide metal pieces that do not meet such metal filling requirements.

II. Basic Design Concept

The most common metal filling rules that many foundries enforce include a) filling empty areas with a minimum metal density, and b) introducing random holes in large metallic pieces so the metal density does not exceed a preset limit [5-7]. This random hole pattern is usually referred to as the "cheese" pattern. Generation of the "cheese pattern" considerably increases the mask computational process time leading to an increased production cost. In addition, the circuit designer is almost never aware of the post-design "cheese" pattern rules leading to an inherent uncertainty in the circuit performance. Furthermore, the algorithm that generates the cheese pattern changes over time to increase the production efficiency. As a result, the fill and "cheese" patterns disturb the layout geometry randomly leading to an inductor performance subject to the enforced CMP ratio rules.

This paper addresses these issues by introducing a new inductor type (strip-patterned inductor) that actively engages the metal density rules. Fig. 1 shows the layout of such a design and compares it with a conventional single-line inductor with the "cheese" filling pattern. The strip-patterned inductor consists of 7 narrow strips with spacing between them. Each strip width is 4μm and the spacing is 1μm. The single-line inductor consists of one 34μm-wide metal line that is patterned by BEOL metal density rule. It is important to note that no such rule is needed for the strip-patterned inductor. In the diagram, 80% maximum metal density is enforced by the patterns. Both inductors' layout widths are 34μm, and the center line length is about 1000μm.

As it can be observed the strip-patterned inductor a) eliminates the need for the "cheese" pattern metal filling rule;

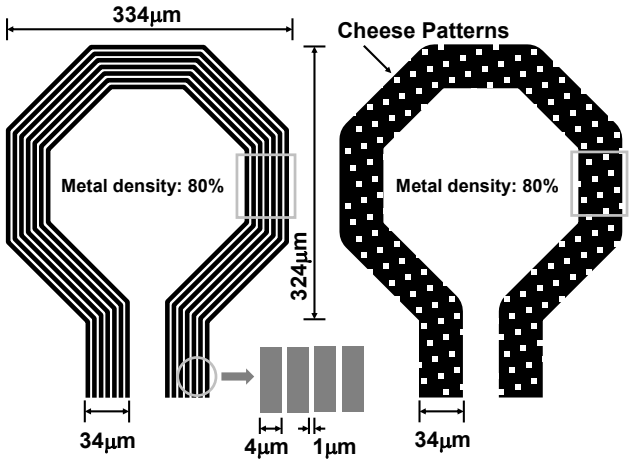


Fig. 1. The proposed strip-patterned inductor (left) and a conventional single-line inductor with the "cheese" filling pattern (right). The geometrical details are given in the text for both inductors.

b) significantly reduces the mask computational processing time leading to reduced manufacturing cost; c) allows the designer to maintain a better control on the final circuit performance by removing processing uncertainties; d) maintains a quality factor equally high or slightly better than state-of-the-art designs. We support this design by measurements and simulations that compare the proposed strip-patterned inductor to the conventional single-line inductor implementation in a 65nm SOI technology. Additionally, we demonstrate efficient full-wave inductor models that accurately predict the strip-patterned inductor performance in the presence of parasitic floating filling metals.

III. Strip-Patterned Inductor Modeling

Fig. 2 shows a simplified cross-section of the layers utilized in the SOI process to build the inductors. In order to accurately analyze the performance of the strip-patterned inductor we employed a commercially available full-wave three-dimensional Finite Element Method (FEM) simulation tool (Ansoft HFSS). Due to the multiple thin layers involved in this process and the large number of dummy metal fills in the fabricated inductors, an FEM model replicating exactly the fabricated structures would be impractical as it would require unreasonably high computational time to analyze it. Instead we follow an alternative approach that involves two steps: a) replace the technology layer and the dummy metal fills underneath the inductor with simplified equivalent layers; and b) replace the dummy fill pattern at the inductor level with a limited number of equivalent strips around the inductor. For the first step floating dummy metal fills between the inductor and SOI are considered. The dummy metal fills increase the inductor parasitic capacitance by effectively shortening the electric field paths due to the highly conductive dummy metals [9-10]. This effect can be treated in simulation by increasing the dielectric constant or reducing dielectric thickness. Considering the very small metal fill dimensions (length and width are both less than 2µm), the effective thickness can be calculated by [10]

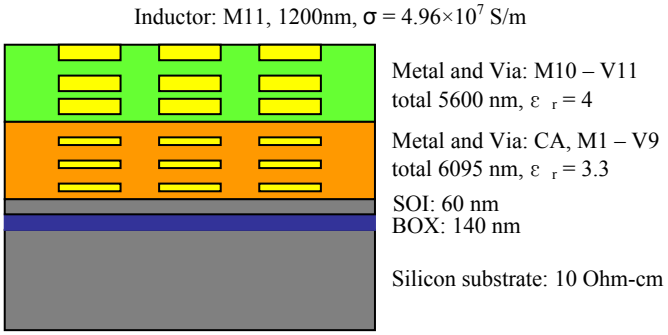


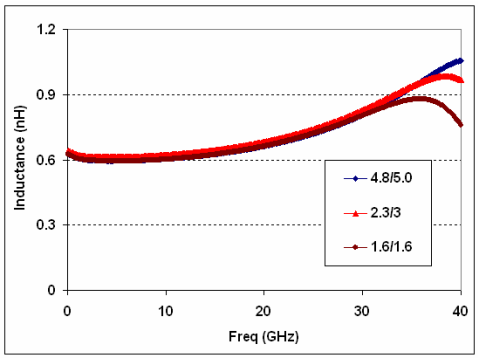
Fig. 2. Brief schematic of layers for fabricated inductors.

$$t_{eff} = t \cdot \max(0, 1 - 2 \cdot FF) \quad (1)$$

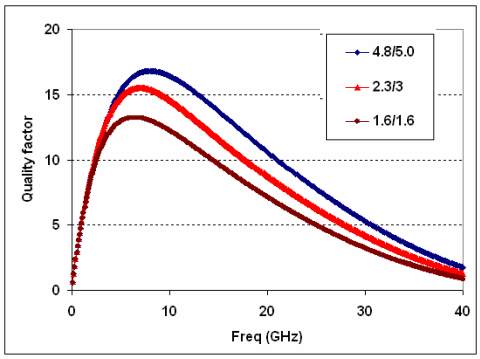
where t is the dielectric layer thickness containing the dummy metal fill and FF is a fill factor, for instance 0.25 for 25% metal fill in our process [10]. This filling factor reduces the effective thicknesses of the SiO_2 and polyimide layers from 5.6 to 4.8µm and from 6.095 to 5.0µm respectively. The effect of this on the inductor value and quality factor can be seen in Fig. 2. While the inductance value remains almost unchanged, the peak Q may drop significantly particularly for high fill factors.

The dummy metal fills around the inductor deteriorate the inductor loss due to eddy current effects and increase its series resistance [6-7]. As described in [6], dummy metal fills inside and outside the inductor cannot be neglected for a single turn inductor at high frequencies. At the same time they cannot be directly modeled in a FEM due to their large number. Thus we need to employ effective loss techniques to replace the small dummy metal shapes with a simpler structure.

The first approach we considered is shown in Fig. 4. We generated horse-shoe-shape dummy metal fill inside and outside close to inductor instead of small square dummy metal fills. We found that three floating lines inside the inductor and



(a)



(b)

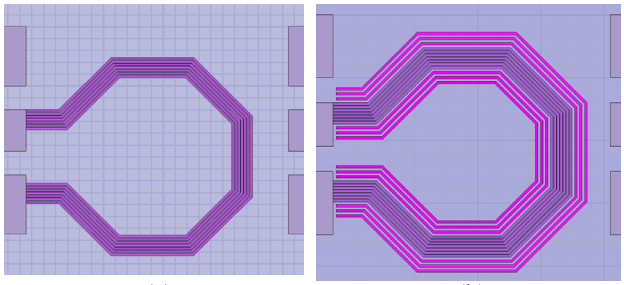
Fig. 3. Impact of effective dielectric layer thickness (see equation 1) in (a) inductance and (b) quality factor values. The original SiO_2 and polyimide thicknesses are 5.6 and 6.095µm respectively. For the 25% filling factor in the considered fabrication process these thicknesses become of 4.8 and 5.0µm respectively.

three outside it give adequate accuracy. This approximation is based on the assumption that most of the eddy current loss is caused by current flowing on the metal fills closest to the inductor. By connecting these metal fills we overestimate this loss. However, this is approximately balanced by ignoring the current on further metal square fills. Fig. 5 shows the impact of this method on the inductor quality factor. As it can be observed, the peak Q in this modeling approach drops by about 20% due to the metal fill effect at the inductor layer.

A second approach was also attempted in order to further reduce the computation time. In this approach we considered an arbitrary conductivity in the polyimide layer (CA, M1-V9) to simply increase high frequency loss. As Fig. 5 shows, the value of 10S/m provided results very close to the first approach (horse-shoe-shape dummy metal fill). While this is a less intuitive approach and does require a one-time curve-fitting to find the optimum fictitious conductivity value, it has the advantage of decreasing the simulation time by 7-20× depending on the geometry.

IV. Fabrication and Measurements

The strip-patterned inductor and single-line inductor shown in Fig. 1 were fabricated on the top copper layer of the 65nm SOI technology. As we mentioned in Section I, the "cheese" patterning that is only necessary for the single-line inductor is not scalable, and it is random in the sense that a designer might not be aware of the patterning algorithm along other nearby structures. The strip-patterned inductor's total effective metal line width is 28µm. Considering a 1.2µm top metal layer thickness, the conducting metal cross section areas are



(a) (b)

Fig. 4. Modeling technique to account for the dummy metal fills at the inductor layer. (a) Strip-patterned inductor without dummy metal fill pattern. (b) Strip-patterned inductor with horse-shoe dummy metal fill pattern. This approximates the real pattern by assuming that most of the eddy current flows immediately next to the inductor.

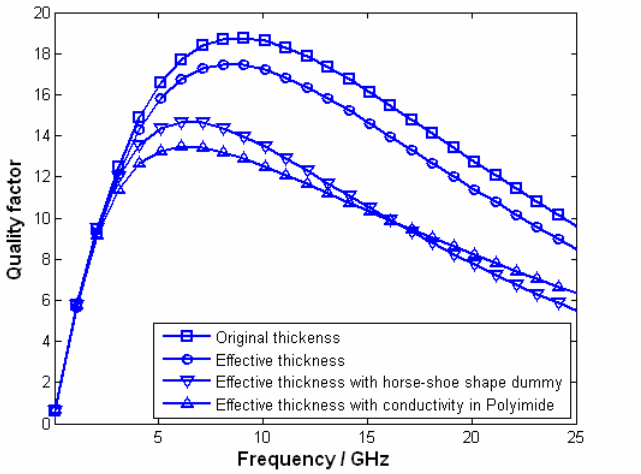
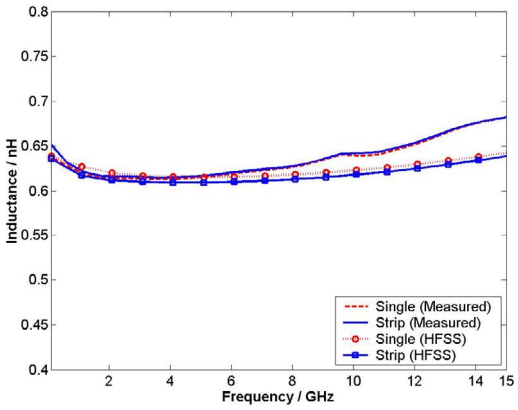


Fig. 5. Summarized impact of dummy metal fills in the dielectric layers and on the inductor layer. The square (□) shape shows the inductor quality factor if both effects are neglected. The circle (o) shape accounts for the metal fills in the dielectric layers underneath the inductor. The reverse triangle (∨) shape accounts for both effects using the horse-shoe model for the metal fills at the inductor layer. The triangle shape (∧) accounts for both effects but models the metal fills at the inductor layer by assuming an effective polyimide conductivity of 10S/m.

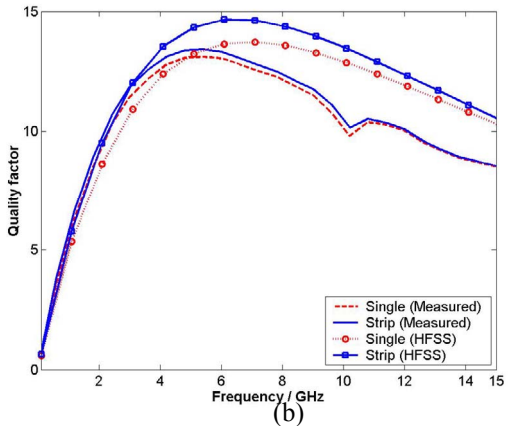
33.6µm^2 for the strip-patterned and 40.8µm^2 for the single-line inductor. The inductors' conducting surface boundaries are 72.8µm for the strip-patterned and 70.4µm for the single-line inductor.

The implemented inductors' 1-port S-parameters were measured from 50MHz to 15GHz using standard calibration and open-short de-embedding schemes. Their measured inductances are 0.617nH and 0.615nH at 5GHz as plotted in Fig. 6. As expected, the layout dimensions of Fig. 1 resulted in similar inductances for both inductors. The strip-patterned inductor peak Q is 13.46 and the single-line inductor peak Q is 13.17. When 74 pairs of inductors from a 300mm wafer are measured, the same trends are observed as plotted in Fig. 7. In average, self-resonant frequencies are at 5.6GHz, and the Q-factors are 13.02 for the strip-patterned and 12.77 for the single-line inductor. Also, Q-factor 1σ variations are 2.09% for the strip-patterned and 2.23% for the single-line inductors at 5.6GHz. Both numbers suggest BEOL process variation is under control. As expected, the striped inductor has slightly less variation than the single-line design.

For both inductors we also plot in Fig. 6 the simulated results based on the models discussed in Section III. The



(a)



(b)

Fig. 6. Measured and simulated results for both the strip-patterned and the single-line inductor. The presented models agree very well with measurements for both cases. The loss model used for both inductors follows the second approach where the polyimide layer conductivity is assumed as 10S/m (please Fig. 5).

second approach (polyimide conductivity of 10 S/m) has been followed for modeling the dummy metal fill at the inductor layer. The very good agreement observed between simulations and measurement for both inductors underline the fact that the models are physically meaningful.

V. Conclusion

A new strip-patterned inductor is presented whose design actively engages metal fill rules. This results in reduced manufacturing cost and process reduced uncertainties because of the simplified dummy fill masks. At the same time maintains state-of-the-art performance, comparable with conventional designs. The proposed structure is demonstrated in a 65nm SOI process. Efficient modeling techniques are also

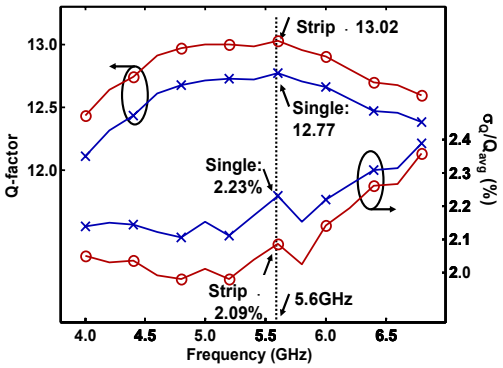


Fig.7. Statistical measurement plots of inductor Q-factors. The strip-patterned inductor has Q-factor of 13.02 and the single-line inductor has 12.77 on average at 5.6GHz. The 1σ variations are 2.23% for the strip-patterned and 2.09% for the single-line inductor.

demonstrated for taking into account the dummy metal filling in all significant layers.

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