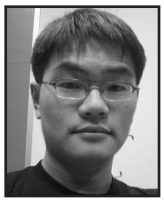
## 30.3 Performance Variability of a 90GHz Static CML Frequency Divider in 65nm SOI CMOS

**Daihyun Lim[1], Jonghae Kim[2], Jean-Olivier Plouchart[2], Choongyeun Cho[2], Daeik Kim[2], Robert Trzcinski[2], Duane Boning[1]**

[1]Massachusetts Institute of Technology, Cambridge, MA, [2]IBM, Hopewell Junction, NY



D. Lim

A static CML divide-by-2 frequency divider is integrated in 65nm SOI CMOS. The maximum operating frequency is 90GHz while dissipating 52.4mW. The self-oscillation frequency is 92GHz with 0.57pJ switching energy. Measurement of self-oscillation frequency at multiple bias conditions enables estimation of the variation in threshold voltage, capacitance, and resistance.

*See Digest page 542*

### Outline

- Motivation
- Design of a mm-Wave Static CML Frequency Divider in 65nm SOI CMOS
- Implementation & Measurement
- Extraction of Circuit Parameter Variability
- Conclusion

### Design of Frequency Divider

**Design concerns:**

*A. Bandwidth:*

$$f_{SO} \approx \frac{g_{m,Diff}}{2\pi \cdot C_{P,tot}} \approx \frac{1}{2\pi \cdot R_L C_{P,tot}} > 30\,\text{GHz}$$

$$C_{P,tot} = C_{Diff} + C_L + C_{R_L} + C_W \approx 20\,\text{fF}$$

*B. Voltage swing:*

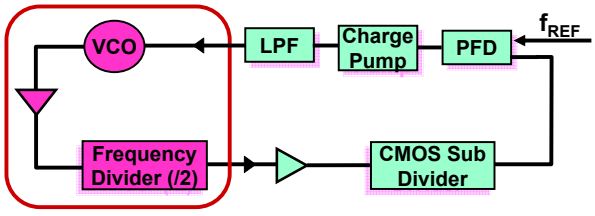
$$SW = R_L C_{P-P} > 1\text{V}_{\text{P-P}}$$

$$R \approx 230\Omega$$

*C. Inductive peaking:*

$$L = \frac{R_L^2 C_{P,tot}}{3.1} \approx 330\,\text{pH}$$

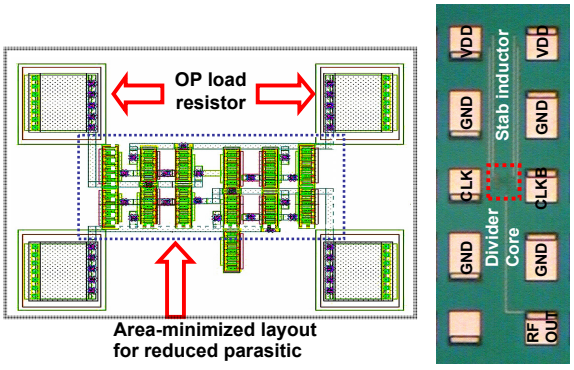
### Motivation



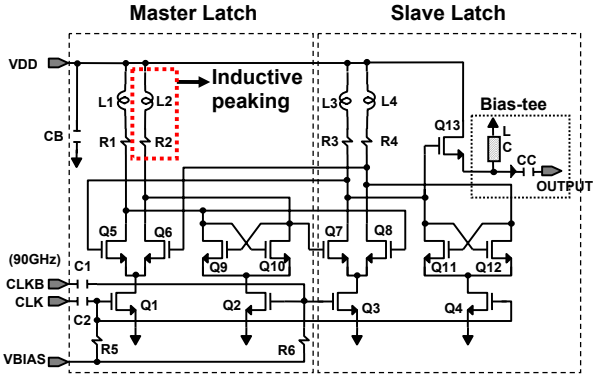

- Reduced VCO tuning range
- Signal power loss through interconnect
- Reduced operation range of frequency divider

➡ Process variation of the frequency divider must be carefully considered in an early design stage.

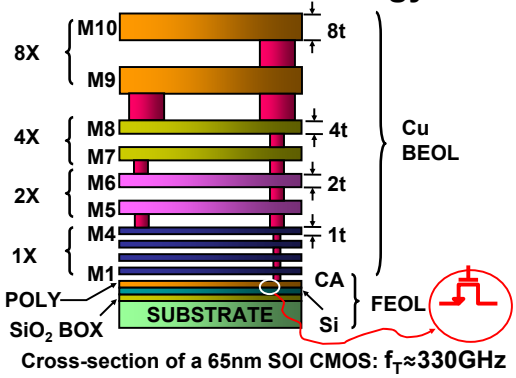
### Layout and Die Photo




### Divider Schematic



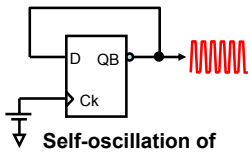

### Selected Technology



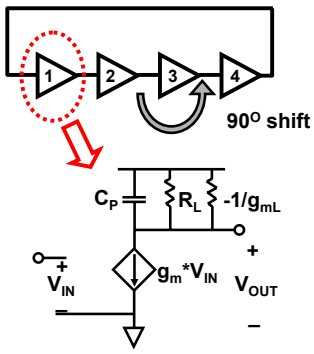

Cross-section of a 65nm SOI CMOS: $f_T \approx 330$GHz

## Self-Oscillation of Frequency Divider




Self-oscillation of Frequency Divider




$$\omega_{SO} = \sqrt[4]{\frac{g_{m1}g_{m2}g_{m3}g_{m4}}{C_{p1}C_{p2}C_{p3}C_{p4}}} \approx \frac{1}{R_L C_P}\frac{g_{mD}}{g_{mL}}$$

## Back-Propagation-of-Variation

$$\Delta f_{SO} = \alpha \cdot \Delta V_{TH} + \beta \cdot \Delta R_l + \gamma \cdot \Delta C_l$$

Frequency deviation as a linear combination of parameter deviation

$$\alpha = f_1(V_{BIAS}, V_{DD})$$
$$\beta = f_2(V_{BIAS}, V_{DD})$$
$$\gamma = f_3(V_{BIAS}, V_{DD})$$

Sensitivity is a function of bias conditions.

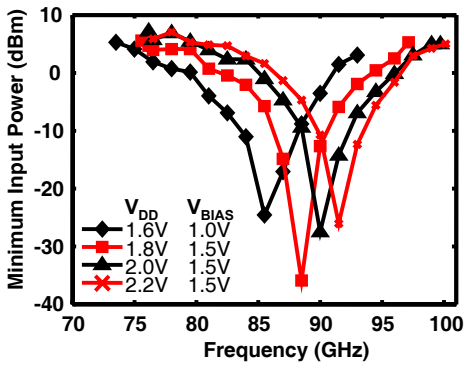
$$\begin{bmatrix}\Delta f_{SO1}\\ \Delta f_{SO2}\\ \Delta f_{SO3}\end{bmatrix} = \begin{bmatrix}\alpha_{BC1} & \beta_{BC1} & \gamma_{BC1}\\ \alpha_{BC2} & \beta_{BC2} & \gamma_{BC2}\\ \alpha_{BC3} & \beta_{BC3} & \gamma_{BC3}\end{bmatrix} \cdot \begin{bmatrix}\Delta V_{TH}\\ \Delta R_l\\ \Delta C_l\end{bmatrix} = S \cdot \begin{bmatrix}\Delta V_{TH}\\ \Delta R_l\\ \Delta C_l\end{bmatrix}$$

Sensitivity is calculated from circuit simulation with nominal parameters.

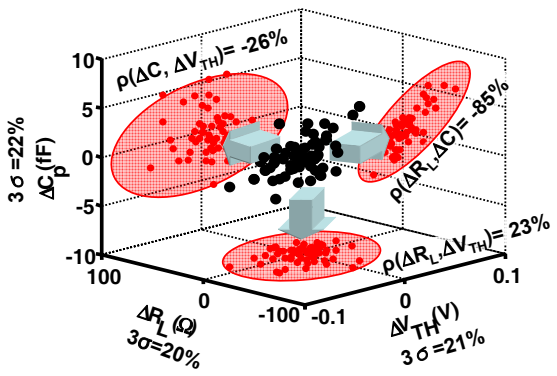
$$S^{-1} \cdot \begin{bmatrix}\Delta f_{SO1}\\ \Delta f_{SO2}\\ \Delta f_{SO3}\end{bmatrix} = \begin{bmatrix}\Delta V_{TH}\\ \Delta R_l\\ \Delta C_l\end{bmatrix}$$

Pseudo-Inversion of sensitivity matrix

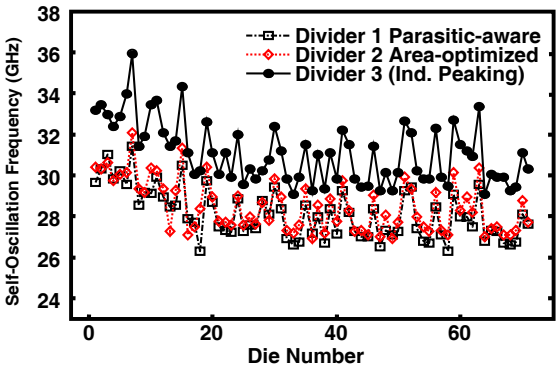
## Input Sensitivity Curves




## Correlation Between Circuit Parameters




## Inductive Peaking and Layout Alternatives




## Summary & Conclusion

- A 90GHz 2:1 static CML frequency divider is implemented in 65nm SOI CMOS.
- The divider operates up to 100.2GHz for a 4.87dBm differential input with 52.4mW.
- Process variation is highly systematic across a wafer with more than 90% cross correlation between wafers.
- The variation of circuit parameters and their correlation are estimated using the sensitivity analysis.

## Systematic Wafer-to-Wafer Variation