30.3 Performance Variability of a 90GHz Static CML Frequency Divider in 65nm SOI CMOS

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A frequency divider is an essential and critical building block in high-performance clock synthesizers. Since the frequency divider operates at the highest frequency in the system in order to pre-scale the high-frequency VCO output, the divider speed and power trade-off should be carefully considered at an early design stage. In particular, above 50GHz, the input power reaching the frequency divider is significantly reduced by the parasitic interconnect capacitance and resistance. For limited input power, the operating range of the frequency divider is thus narrowed but must still cover the tuning range of the VCO for proper operation of the clock synthesizer. In addition to nominal speed, power and operating-range requirements, variability in the frequency divider is a critical issue for the manufacturing yield of high-speed clock synthesizers. Recently, 21.5% (3σ) variation in the maximum operating frequency of dividers over a wafer in 90nm SOI technology has been reported [1]. In this paper, a static CML frequency divider is implemented in 65nm SOI CMOS technology to achieve 100GHz maximum operating frequency with 52.4mW power dissipation. Across-wafer and wafer-to-wafer variations of the divider self-oscillation frequency are measured at 80 different bias conditions using 2409 divider samples (3 divider types on each of 73 dies, for 11 wafers). The variation of critical circuit parameters for divider performance including threshold voltage, parasitic capacitance and resistance is estimated using the measurement data and sensitivity analysis at different bias conditions.

Figure 30.3.1 shows the schematic of a 2:1 static frequency divider. The divider uses CML master and slave latches with inductive peaking for bandwidth enhancement. The operating range of the frequency divider is designed to be centred at 80GHz. The bottom transistors (Q1-Q4) are sized to 10μm to drive up to 10mA current. The size of the latch transistors (Q9-Q12) is adjusted to 8μm to reduce capacitive loading at output nodes while satisfying the self-oscillation condition $g_{mL}R_L>1$ [3] with poly-silicon resistor loads. Four 300pH high-Q stab inductors are introduced to increase the bandwidth by cancelling parasitic capacitance.

Figure 30.3.2 shows the sensitivity curves of the frequency divider at 4 different bias conditions, indicating the input power required to achieve 2:1 frequency division at a given input frequency. Based on the frequency-range limitation of the equipment used in this measurement, the divider is biased to work over the input frequency range from 75 to 110GHz. The divider biased at 2.2V V_{DD} and 1.5V V_{BIAS} operates up to 100.2GHz for a 4.87dBm differential input. This is a 1.52× improvement in frequency performance over the fastest reported static frequency divider in 90nm SOI CMOS [1]. A minimum input power point is achieved at 92GHz that corresponds to a 46GHz self-oscillation frequency. The power consumption is 52.4mW and the switching energy at the self-oscillation frequency is 0.57pJ that is more than 42% reduction compared to other static frequency dividers achieving 100GHz maximum frequency in various technologies [4, 6-9]. A higher V_{DD} increases the self-oscillation and maximum operating frequency, but the operating range does not change significantly. For a small input swing, the static frequency divider can be analyzed as an injection-locking oscillator, and smaller bias current (lower V_{BIAS}) gives a wider operating range [2]. Thus, the operating range of this divider can be dynamically adjusted to the tuning range of a VCO by changing V_{DD} and V_{BIAS}.

For functional yield and performance variation analysis, measuring the maximum operating frequency (F_{MAX}) is important. However, the F_{MAX} measurement is costly since it requires mm-wave frequency sweeps and the detection of proper division. In contrast, the self-oscillation frequency is more efficient to measure and the F_{MAX} tracks the self-oscillation frequency [1, 4]. Figure 30.3.3 shows the process variation of self-oscillation frequency when

V_{DD}=1.8V and V_{BIAS}=1.5V across a wafer. Divider 1 and divider 2 are identically sized, but divider 2 has more compact placement and routing for decreased wire capacitance. Divider 3 has inductive peaking in addition to the layout of divider 2. For the 3 different types of dividers, the self-oscillation frequency measurements show 3σ of 16.7% and a 22% range between the fastest and slowest dies. In Fig. 30.3.3, divider 2 shows a 0.39GHz average improvement compared to divider 1 due to layout optimization. The inductive peaking in divider 3 results in a larger and consistent 2.57GHz average increase compared to divider 2.

While the across-wafer variation of the self-oscillation frequency is 16.7% (3σ), the variation pattern across a wafer is highly systematic. Figure 30.3.4 shows the within-wafer variation for 11 different wafers at a fixed bias condition (V_{DD}=1.8V and V_{BIAS} =1.5V). Each wafer shows a similar pattern of within-wafer variation with a parallel shift: the cross correlation between different wafers is 92% on average. Based on this result, with a pre-characterized profile of a reference wafer, the performance of all dies in a random wafer can be estimated with 1.5% average error by measuring a single die and checking the difference with the reference wafer profile. Figure 30.3.5 depicts the distributions of self-oscillation frequency for each wafer based on Gaussian assumption. For the variation in wafer-processing environment, the mean value of each wafer spreads from 29.9 to 35.8GHz, and 3σ of each wafer changes from 15% to 18%. Considering all 803 dies, 3σ total variation (within-wafer and wafer-to-wafer combined) is 23.8%.

The major circuit parameters impacting the self-oscillation frequency are bias current, parasitic capacitance, and load resistance. The bias current is a strong function of the threshold voltage of input transistors. By simulation, the sensitivity of the self-oscillation frequency with respect to the change of the threshold voltage, parasitic capacitance, and load resistance can be calculated at different bias conditions. Based on a first-order performance fluctuation model, the deviation of the circuit parameters from their nominal values can be calculated using the sensitivities and the measurement data of self-oscillation frequency at 9 different bias conditions with a back-propagation of variance technique [5]. The extracted 3σ of threshold voltage, parasitic capacitance, and resistance variation is 21%, 22% and 20%, respectively. For accurate Monte Carlo analysis of circuits using the same process, knowing the correlation between the circuit parameters is essential. The scattering plot in Fig. 30.3.6 shows a significant negative correlation (ρ=-0.85) between parasitic capacitance and resistance. The threshold voltage does not show notable correlation with other parameters. The chip micrograph of the divider circuit is shown in Fig. 30.3.7.

References:
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Q1-Q8: W/L=10μm/65nm
Q9-Q12: W/L=8μm/65nm
R1-R4: W/L=8μm/5μm, 230Ω
R5-R6: W/L=8μm/1.25μm, 50Ω
L1-L4: W/L=8μm/300μm, 300pH
C1,C2: 1pF VNCAP
LC: External choke coil
CC: Coupling cap
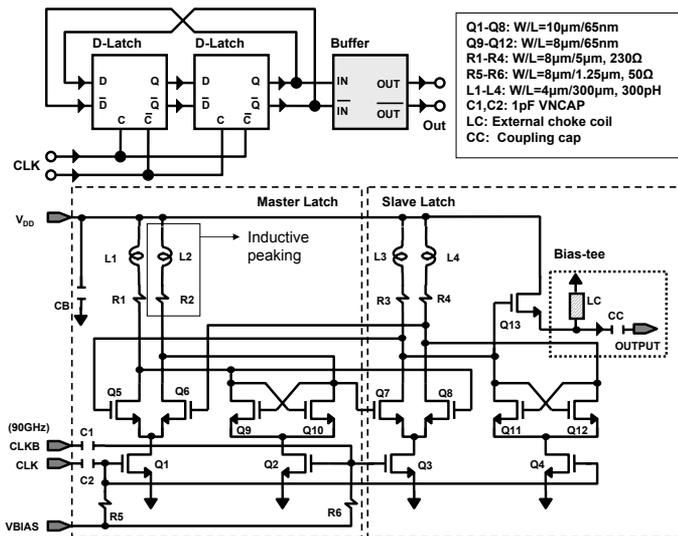
Figure 30.3.1: Schematic of a static CML 2:1 frequency divider with inductive peaking.
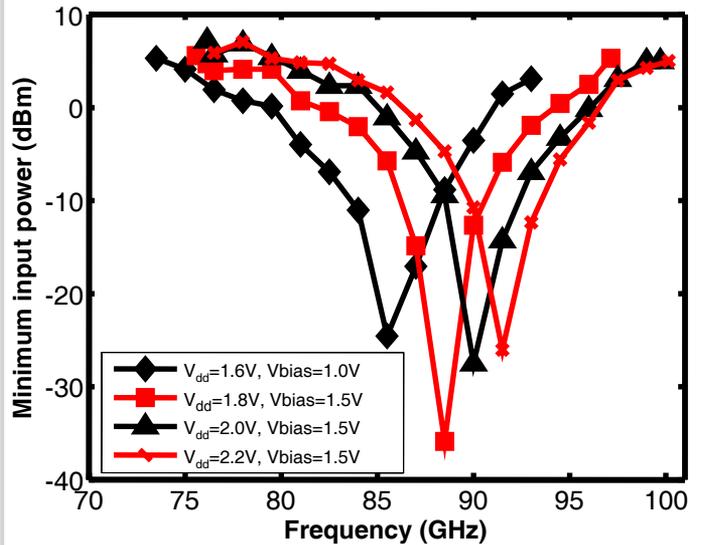
Figure 30.3.2: Input sensitivity at different bias conditions.
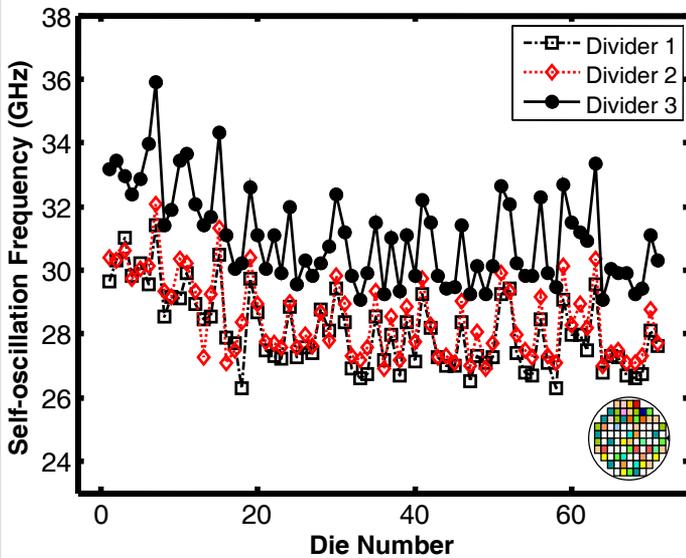
Figure 30.3.3: Variation of self-oscillation frequency w/ and w/o inductive peaking.
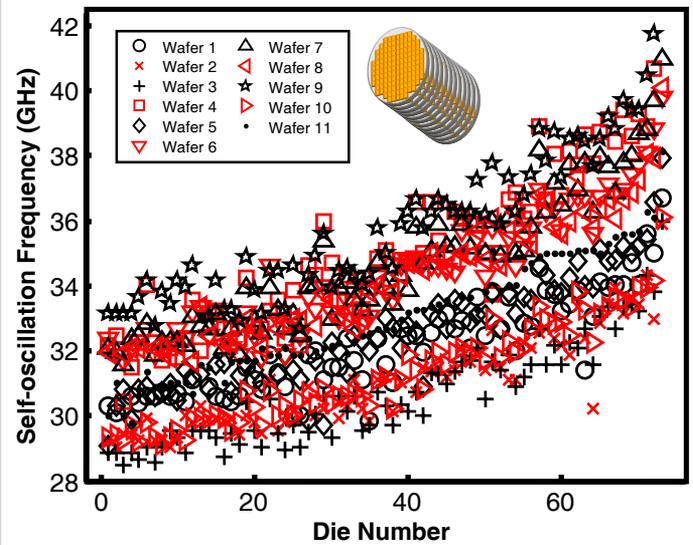
Figure 30.3.4: Wafer-to-wafer variation of self-oscillation frequency.
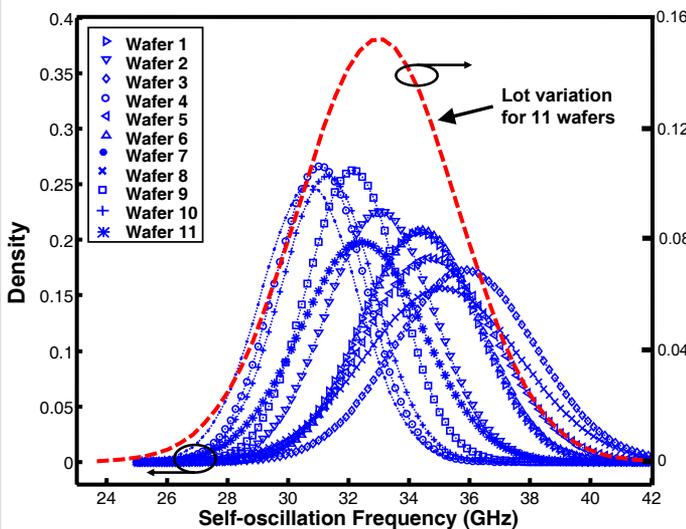
Figure 30.3.5: Distribution of self-oscillation frequency in 11 wafers and total lot variation.
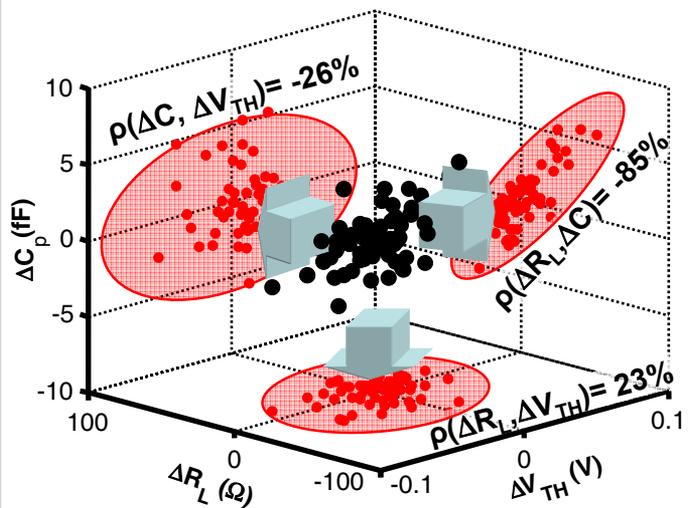
Figure 30.3.6: Correlation between the estimated threshold voltage, parasitic capacitance, and resistance.

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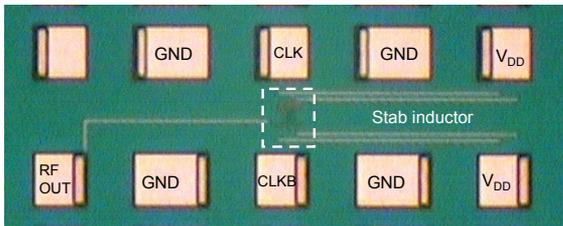
Divider core (20x40µm²) and stab inductors (300x4µm²)
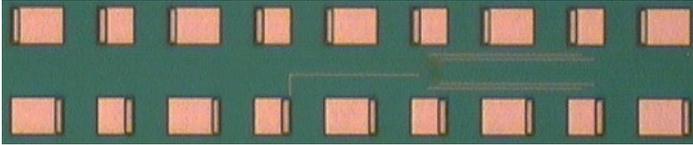
Divider with wedge pad-sets (dimension: 1.3x0.5mm²)

Figure 30.3.7: Chip die micrograph.