A 5 GHz 11-Stage CML VCO with 40% Frequency Tuning in 0.13μm SOI CMOS

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***Abstract*—This paper presents a manufacturable CML-based 11-stage VCO for digital system clock fabricated in 0.13μm SOI CMOS. The 11-stage design enables quality oscillation, wide frequency tuning range, and process variability rejection. On average, the VCO exhibits 40% frequency tuning range from 4.23 to 6.35GHz. The VCO phase noise is -129.8dBc/Hz at 10MHz offset in current-controlled measurements, and average FoMT(10%) is -178.1dBc/Hz. Full 200mm wafer scan result is presented along the phase noise measurement to demonstrate a statistical methodology.**

I. Introduction

A quality clock signal generation with standard-based specification becomes challenging, as the digital system adds complexity with multi-core architecture. Not only the high-performance microprocessors, but also low-power and mobile platform seeks similar trend for multi-media data processing. Processor core-to-core communication, internal memory access, and external I/O necessitate high-speed and quality clocking for system synchronization and data integrity. A PLL and a VCO in it determines the clock frequency tuning range (FTR) and phase noise (PN). Having a wide FTR improves chip-limited yield (CLY) through process variation rejection when the oscillation frequency is centered well. Ideally, with a 50% FTR, the VCO can tune to all the frequencies below the maximum frequency. The clock signal quality is measured with PN in frequency domain and jitter in time domain. For wide FTR, a current-mode logic (CML) delay cell is used for digital systems, while an LC resonator is common for high-quality communication system clock.

CML-based VCO design relies on the front-end-of-the-line (FEOL) models, and they are easier to develop in early technology stage. Model immaturity might be ignored, since a CML VCO usually has wide FTR up to 50%. As long as it has high enough oscillation frequency, it can tune to lower frequency range with frequency division. Therefore PLL CLY would be overcome. One of the drawbacks is marginal PN performance, worse than LC VCOs. Until recently, CML VCOs design efforts have addressed maximum oscillation frequency and tuning range. There are several ways to improve PN, but the FEOL high-speed performance has not been enough for those techniques. A simple approach to improve PN is to have a multiple-stage oscillator for larger output swing, than 1-, 2-, or 3-stage VCOs. It is feasible when FEOL device becomes much faster than the design frequency. SOI CMOS technology offers performance gain over bulk CMOS by reducing parasitic capacitance in the source and drain diffusions. Also due to high-resistive substrate, it is attractive as a high-performance RF SoC design platform. The other advantage of multiple-stage VCO design is the rejection of process variability in scaled CMOS process through averaging. The CML VCO design should be examined and qualified statistically in important performance parameters, such FTR and PN, as described in Fig. 1. The model-to-hardware correlation and circuit design feedback are subject to such observations.

This paper presents a 11-stage CML VCO design (II), test setup (III), and statistical measurements (IV). The VCO demonstrates wide FTR and state-of-the-art FoMT. Also statistical analysis reveals the 11-stage design process variation rejection compared with a 3-stage design, and PN variation model.

II. 11-stage CML VCO Design

The CML VCO design is intended for a digital system PLL in a RF SoC. Assuming a separate PLL division for digital clocking, target oscillation frequency is 5GHz with 50% FTR. The PN gain is obtained as a trade off between the oscillation frequency and the PN. A simulation shows that the engaged 0.13μm SOI allows 11-stage for 5GHz oscillation. A CML stage is a differential pair with resistive load and inductive load for peaking as shown in Fig. 2. It will expedite logic state

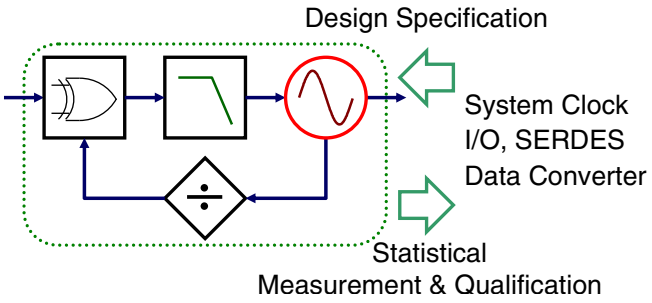

Fig. 1. A block and design flow diagram for digital system clock generation PLL. The VCO and PLL performance requirements are raised as the digital system complexity increases with multi-core microprocessor architecture. The core-to-core clock synchronization, inter-core communication, and external I/O pose stringent clock specifications, while the design has to overcome the process variation in multiple performance parameters.

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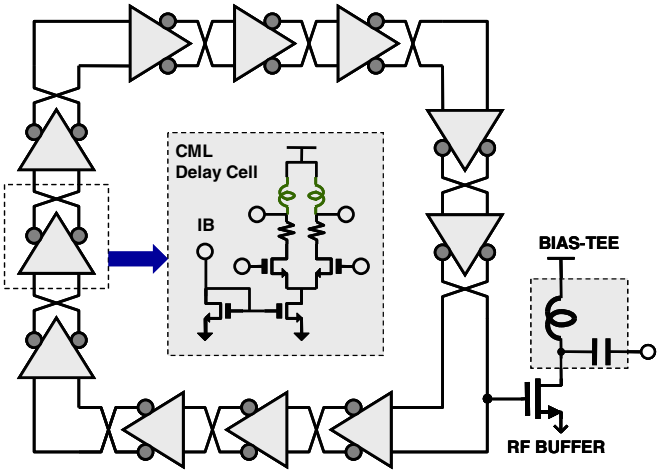

Fig. 2. A schematic diagram of 11-stage CML VCO implemented in 0.13μm SOI CMOS. The number of stages and the target oscillation frequency should be arranged for frequency tuning and PN performance. The multiple stages enhance process variability rejection through averaging. Wide tuning range becomes an important requirement for SoC digital system yield, and the PN should be qualified statistically to meet the demanding standards.

transition, and therefore it improves PN performance [1]. By having 11 CML stages, the process variation is filtered. Since the variation depends on the local and global layout, and chip position in a wafer, it is difficult to model such variations properly. But the multiple-stage averaging will reject both the local and global variation [2].

The circuit design involves several testability issues: 1) RF and DC interfaces, 2) pad pitch and size, 3) probe set, 4) RF buffer circuit, 5) on/off-chip DC decoupling, 6) cable connection, 7) measurement equipment and system, and 8) automated test procedure. Especially, RF buffer and DC decoupling are important for PN and FoM measurements. It is because the DUT is surrounded and connected to noise sources, such as DC source-and-measurement unit (SMU), control PC, and wafer stepper. As shown in the chip photograph Fig. 3, there are 2 DC inputs and 1 RF output, and 150μm-pitch pad and probe set are used. A common source RF buffer was added to improve output signal power, and vertical native capacitors were added to the layout extensively, to remove noise from power sources. The VCO is testable at M3 level, and it reduces the RF design-for-testing cycle time for circuit debugging.

III. Test Setup and Functional Verification

The information on the test setup is used in the design stage, to make sure that the RF output matches the external test environment. The simulation and instrument specifications are brought together to see if they meet the circuit performance. Estimated signal losses in on-chip connection, probe contact resistance, probe set, cable, and bias-tee should be considered in design and test setup. An in-house automated test code is used, and the test conditions are manually set based on the simulation and nominal measurements. Fig. 4 shows a test setup diagram for the VCO. DC SMUs provide operating condition to the VCO through cable and probe set. The probe set is held by a wafer tester, and the tester performs robotic

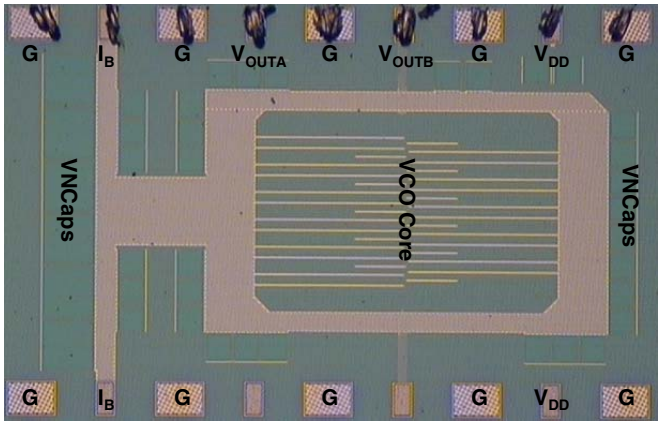

Fig. 3. Fabricated chip die photograph. The VCO core is extended by slab inductors, power grid, and decoupling vertical native capacitors (VNCap). The VNCap is heavily populated for DC signals – I_B and V_{DD}. Padset is 150-μm 9-pin wedge probe set.

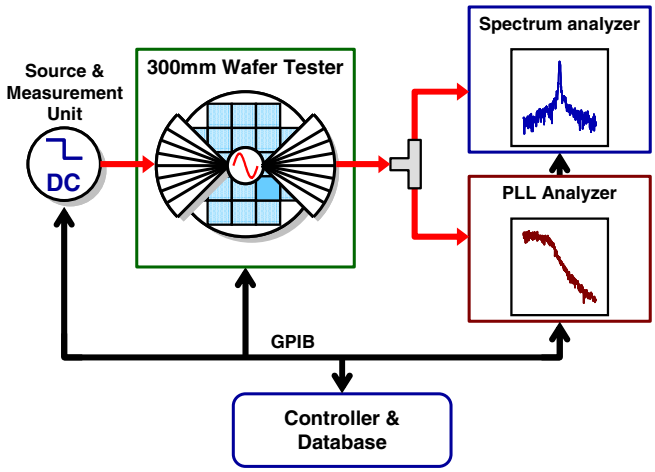

Fig. 4. CML VCO measurement setup diagram. For automated statistical measurement, all instruments including wafer stepper are connected through GPIB. The spectrum analyzer is engaged with a two-step zooming by 5% around the initial peak for measurement accuracy. The spectrum analyzer and the PLL analyzer are synchronized closely to minimize the time difference. For simplicity, the VCO is controlled by the bias current I_B.

movements across the wafer. The RF output is collected by the RF probe and bias-tee. The power splitter divides the signal to spectrum analyzer and PLL analyzer. The PLL analyzer shows faster and more accurate PN measurement in real time than the spectrum analyzer. The spectrum analyzer is used for signal verification and oscillation frequency measurement. All the instruments are connected through GPIB, and the controlling PC provides orchestrated instrument operations. The measurements are transferred to the PC and their validity is evaluated with algorithms based on the VCO spectrum and PN models. For example, an accurate oscillation frequency is reliably determined by a two-step zooming. The test results are recorded in a database that contains lot, wafer, chip site information, test conditions, and measurement results.

The measured VCO output spectrum and PN screen captures are in Fig. 5. The test shows that the VCO and the test setup are functional. Also the PN plot does not show noticeable

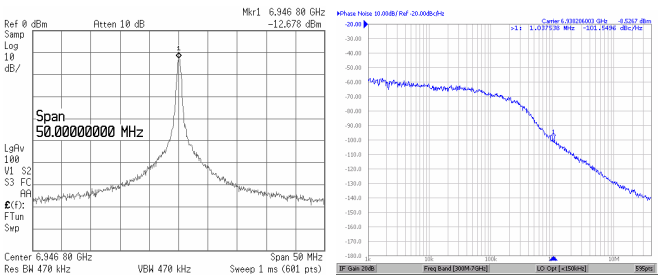

Fig. 5. Screen captures of VCO output spectrum with 50MHz span from the spectrum analyzer and PN at 6.94GHz from the PLL analyzer. The VCO shows -101.5dBc/Hz at 1MHz offset from 6.94GHz. Both screens were manually captured with averaging for demonstration.

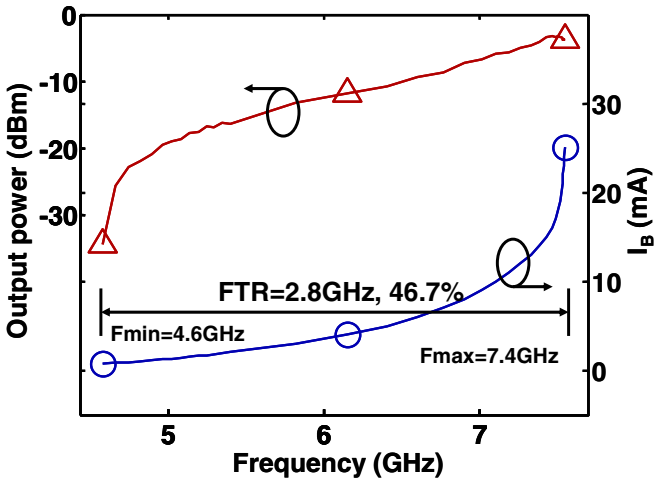

Fig. 6. VCO output frequency for input current I_B and the output signal power. The fastest VCO in the 200mm wafer was measured. The I_B is scanned so that the oscillation frequency is saturated for F_{max}. For F_{min} the I_B is reduced until VCO fails to oscillate. The VCO oscillates from 4.6 to 7.4GHz, with 2.8GHz or 46.7% frequency tuning range.

modulated noise artifacts. In practice, several factors such as the tester condition and global ground should be modified to isolate noise sources. Once the minimal circuit function is verified, a set of repetitive tests are performed, based on the pre-determined test plan. The FTR and the RF output of the VCO are obtained with an automated I_B sweep test code as plotted in Fig. 6. The plots show the implemented VCO output frequency versus input current I_B and RF output power, all sampled with spectrum analyzer. The VCO minimum frequency is 4.6GHz at I_B=1mA, and it tunes up to 7.4GHz at I_B=25mA. The FTR is 2.8GHz, or 46.7% from the center frequency.

IV. Statistical RF Measurement

The other important VCO specification is PN, and the PN measurements with VCO control current I_B sweep are in Fig. 7. The plot shows that PN has regular slope overall. At a lower frequency, the VCO tends to have worse PN in the plot. There are more noises involved near the 1MHz offset in the mid-I_B region. The plot suggests that PN performance should be sampled at the larger offset frequencies of 2, 5, and 10MHz for reliable measurement and comparison. The

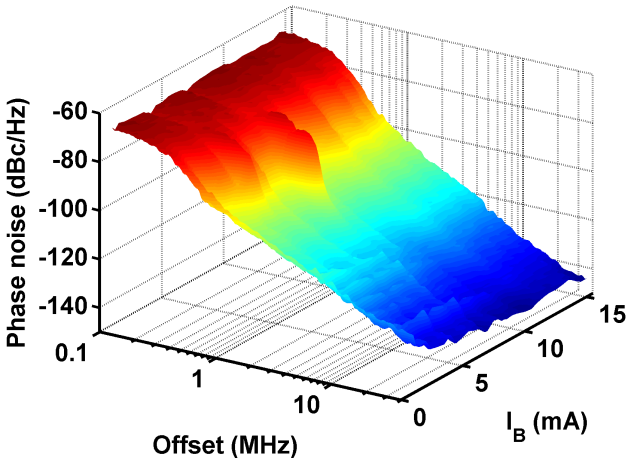

Fig. 7. VCO PN output with input current I_B sweep. Phase noise mechanism changes over the I_B conditions. The PN change is not always monotonic, and there is a bump at a specific I_B condition around 1MHz offset.

plot exhibits that the PLL analyzer noise floor is below the PN at 10MHz, and the PN measurement at 10MHz offset is the VCO PN, not the instrument noise. Also the PN should be measured for both the highest and lowest frequency for the specifications at each frequency, assuming the PN changes monotonically with I_B. The PN measurements tend to have noisy curve, and there is a trade-off between the measurement time and the averaging, with respect to the test scalability. There are several iterations of the test procedure to modify the parameter capturing algorithm, so that the measurements are reliable against variations and anomalies. When confidence is built up in the circuit operation, environment, control, and algorithm, the test set up is qualified for the statistical test.

The test qualification for the statistical measurements will have to proceed with scaled tests on several sites on a wafer, or multiple wafers. It is impossible for an algorithm to be proven error free, and the test system should be qualified based on acceptance criteria. The statistical tests were performed on a 200mm wafer. Fig. 8 shows maximum and minimum tunable frequencies (F_{max} and F_{min}), sorted on the descending FTR. The FTR has good correlation with F_{max} and F_{min}. Using the information and statistics in Table I, the frequency tuning yield of the VCO is estimated. The PN at 10MHz offset with VCO input current I_B=2 and 12mA are plotted against the oscillation frequency in Fig. 9. The PN at I_B=2mA shows stronger fluctuation. Also the PN does not show much correlation to FTR. Still the average and distribution information is used to construct PN yield model. The implemented CML VCO performance is compared in Table II.

V. Conclusion

A 11-stage CML VCO was designed and statistically measured in 0.13μm SOI CMOS. The measurement shows that the VCO has 40% frequency tuning range from 5.3GHz, phase noise of -129.8dBc/Hz at 10MHz offset from F_{max}, and state-of-the-art FoMT(10%) of -178.1dBc/Hz.

TABLE I
CML VCO RF PERFORMANCE STATISTICS

Entity	Average	1-σ (%)	Median	Minimum	Maximum
I_A@F_{max} (mA)	53.2	5.86	53.6	39.8	56.8
I_Q (mA)	1.61	15.8	1.55	1.44	2.85
F_{min} (GHz)	4.23	4.33	4.24	3.83	4.58
F_{max} (GHz)	6.35	5.58	6.35	5.65	7.06
FTR (GHz)	2.12	9.76	2.14	1.71	2.50
FTR (%)	40.0	6.09	40.7	32.5	43.3
P_{RF}@F_{max} (dBm)	-4.40	15.7	-4.24	-6.90	-3.50
Phase noise (dBc/Hz@10MHz,I_B=2mA)	-123.5	2.88	-124.3	-129.5	-113.0
Phase noise (dBc/Hz@10MHz,I_B=12mA)	-129.8	1.20	-129.7	-132.6	-126.9
FoM (dBc/Hz)	-166.1	0.91	-165.9	-169.1	-163.3
FoMT for FTR=10% (dBc/Hz)	-178.1	0.95	-178.3	-181.3	-175.0

TABLE II
PERFORMANCE COMPARISON

Ref	Technology	Type	Frequency (GHz)	Phase noise (dBc/Hz)	Power (mW)	FoMT(dBc/Hz)
[3]	InP HBT	1-stage	13.8 - 21.5	-90@1MHz	80	-169.1
[4]	SiGe	2-stage	18.5 - 25	-105@10MHz	105.6	-162.0
[5]	0.18μm CMOS	3-stage	5.16 - 5.93	-99.5@1MHz	27	-163.3
[6]	0.25μm CMOS	4-stage	4.07 - 5.43	-98.5@1MHz	80	-163.3
This work	0.13μm SOI	11-stage	4.23 - 6.35	-129.8@10MHz	96	-178.1

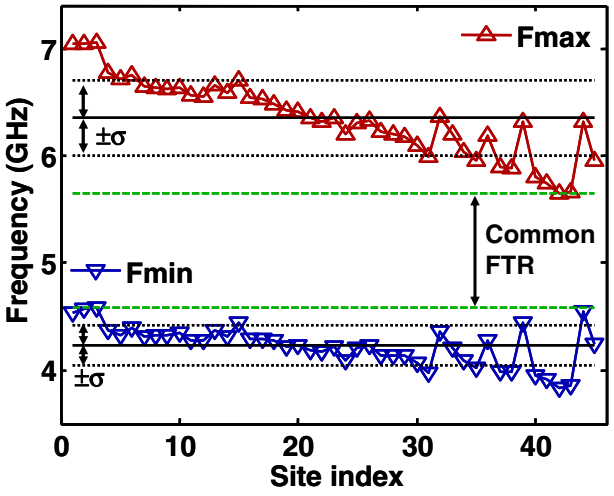

Fig. 8. Statistical measurement on VCO maximum and minimum tunable frequency from a 200mm wafer.

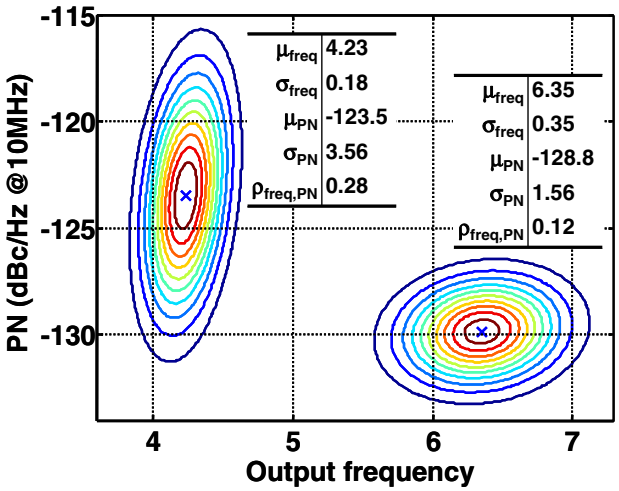

Fig. 9. VCO F_{max} and F_{min} versus PN distribution. F_{min} vs. PN at I_B=2mA shows narrower F_{min} and wider PN variation than F_{max} vs. PN at I_B=12mA.

VI. ACKNOWLEDGMENTS

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