The Process Variability of a V-band LC-VCO in 65nm SOI CMOS

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***Abstract* — The process variability of a V-band LC-VCO implemented in 65nm SOI CMOS is examined. A complementary LC-VCO design, test set up, and measurements are presented. One lot of 300mm wafers are measured for statistics. There are 8 wafers in the lot, and 67 VCOs per wafer. The VCO frequency tuning range statistics, analog variability against digital benchmark, yield estimation, and intra- vs. inter-wafer variations are analyzed and discussed. The VCO average frequency tuning is 63.7-69.6GHz, and it shows 90% yield from 65.1 to 67.9GHz.**

***Index Terms* — Complementary V-band LC-VCO, 65nm SOI CMOS technology, process-induced variation, chip-limited yield, frequency tuning range, inter- and intra-wafer variation.**

I. Introduction

The millimeter wave (mmWave) physical links are emerging to meet the higher-bandwidth communication demands. For SoC integration and manufacturing, CMOS technologies have been sought as design platforms. A sub-100nm CMOS technology is preferred to have high-speed design margins. In addition to the analog design issues such as power efficiency and voltage headroom, the process variability of the advanced CMOS affects the manufacturability [1]. The variability has been studied for digital technology from various perspectives [2]. In the state-of-the-art CMOS, the analog variability has not been thoroughly investigated since the digital technology scaling preoccupies most of development efforts. There is not enough time to establish complicated analog benchmark until the technology is mature for several years. As a result, the analog system becomes a potential limiting factor for chip-limited yield (CLY). An entire SoC chip might fail because the analog system misses the specification, though the digital block is intact. Especially, the VCO's tuning to a desired frequency is the first necessary condition for an mmWave link. As shown in Fig. 1, the mmWave system frequency is much higher than RF, and it is determined by the inductance and capacitance from active, passive, and parasitic devices and components. The parasitic capacitance plays a bigger role as CMOS technology scales down, and the variability becomes more sensitive and complicated. Therefore, frequency tuning range (FTR), centering, variability, and CLY should be considered for a VCO design.

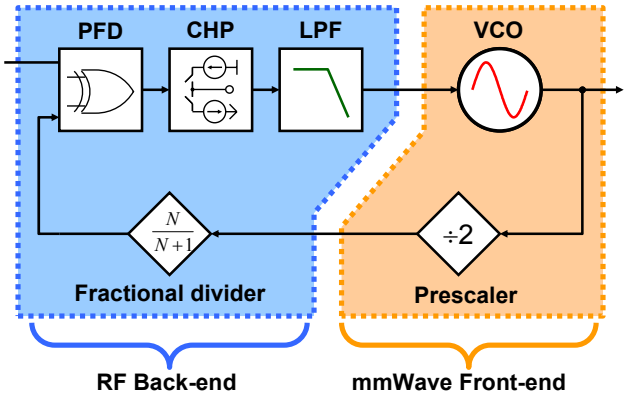

Fig. 1. A mmWave PLL block diagram. The VCO and the prescaler yields are important for the SoC CLY, due to the sub-100nm CMOS process-induced variability in active and passive devices and parasitics.

This paper presents the variability of a V-band LC-VCO in 65nm SOI CMOS. Total 8 wafers in one lot are tested, and there are 67 sites in a 300mm wafer. The CLY of a mmWave system is discussed with the VCO FTR. The VCO design and measurements are described in section II. The statistic observations are discussed in section III. The VCO statistics are analyzed further from the analog benchmark perspectives in section IV.

II. Circuit and Measurement

A complementary LC-VCO in Fig. 2 is implemented for mmWave oscillation in 65nm SOI CMOS. The inverter cross-coupled topology has advantages in phase noise, power consumption, and wide FTR [3].

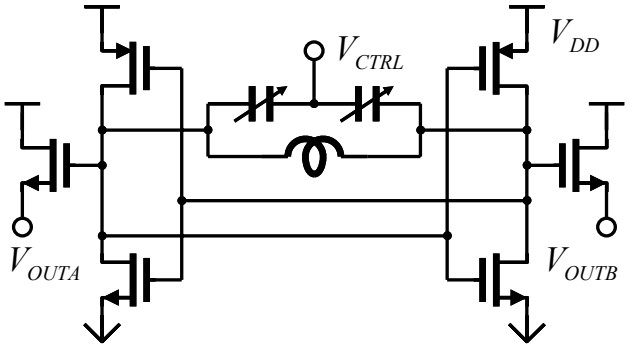

Fig. 2. Complementary inverter cross-coupled LC-VCO schematic diagram.

The topology reveals the technology performance since the PFET f_T , g_m, and the parasitics are not favorable for high-speed oscillation. The PFET f_T and g_m are lower than those of NFET. The PFET width is twice of NFET for output node bias at the middle of supply rails. It will contribute about twice of NFET parasitic capacitance to the output node.

The implemented VCO was tested with an automated 300mm wafer tester shown in Fig. 3. Due to the signal loss in the setup, an LNA is necessary to turn on the V-band mixer. The output signal is amplified to improve the measurement accuracy. The output power level is calibrated at the input of the mixer.

An initial spectrum analyzer span is V-band (50-75GHz), and the VCO output frequency is captured after zooming in on the 2% around the initial peak. A noise floor threshold prevents false peak detection. Power supply is set to V_{DD}=1.2V, and the control voltage V_{CTRL} is swept from 0 to 1.2V with 0.1V step. VCO oscillation frequency is sampled at each condition. One sample takes about 5 seconds. After a circuit is measured, the wafer is stepped to the next chip site. There are 67 chip sites in a 300mm wafer, and 8 wafers in the same lot are repeated for the same measurements. The automation is susceptible to errors. The wafer alignment, wafer thermal expansion, probe alignment, and probe contact resistance will cause measurement errors and data corruption. Most of errors are caught and fixed during the test system qualification.

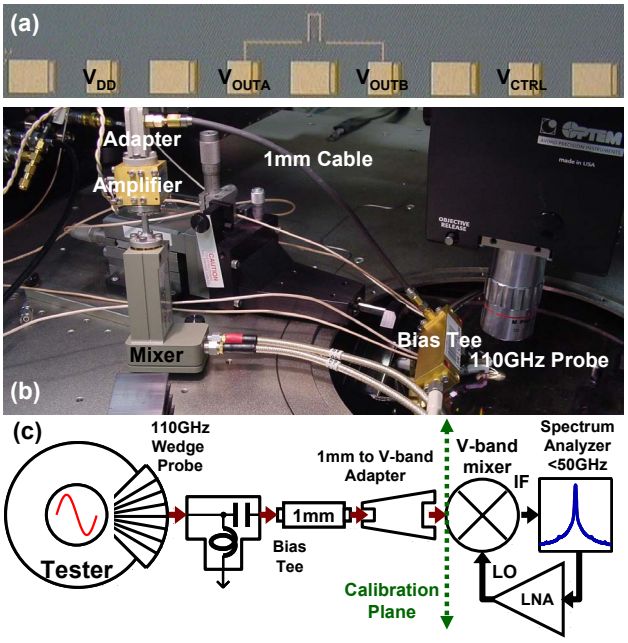

Fig. 3. (a) The implemented V-band LC-VCO chip die photograph, (b) test setup photo, and (c) setup diagram. An amplifier was used to increase test reliability against the spectrum analyzer noise floor.

After the qualification of the automation setup, each case should be examined manually to figure out the cause. For the data presented, the post-automated manual testing was not performed to maintain the scalability of the automated test methodology.

III. VCO Measurement Statistics

The VCO FTR is the main interest for the manufacturability of a mmWave system [4]. The maximum and minimum frequencies of each site on all wafers are plotted in Fig. 4. The plot shows total 536 LC-VCOs' output frequency measurements raw data, and it includes several invalid data points that originate from the measurement error. The VCO frequency ranges from 61.5GHz to 74.9GHz. The VCO FTR is quite wide as much as 8.85% on average. But the minimum of f_{max} (the maximum frequency a VCO tunes) and maximum of f_{min} almost overlap, and the separation is 0.141GHz. It is obvious that the analog process-induced variability would affect the SoC CLY. The circuit should be carefully designed based on the analog device technology benchmark results.

The data are now filtered so that 450 valid VCO data points are used for statistics, as shown in Fig. 5. The filtering conditions are: 1) all V_{CTRL} sweep data points are within 60~75GHz and 2) oscillation frequency increases monotonically with V_{CTRL} sweep. The average FTR is from 63.7-69.6 GHz. The standard deviations from the average are useful to estimate the VCO yield for a desired frequency. In practice, the f_{max} and f_{min} require separate modeling since they have different statistics.

The LC-VCO FTR and oscillation frequencies are

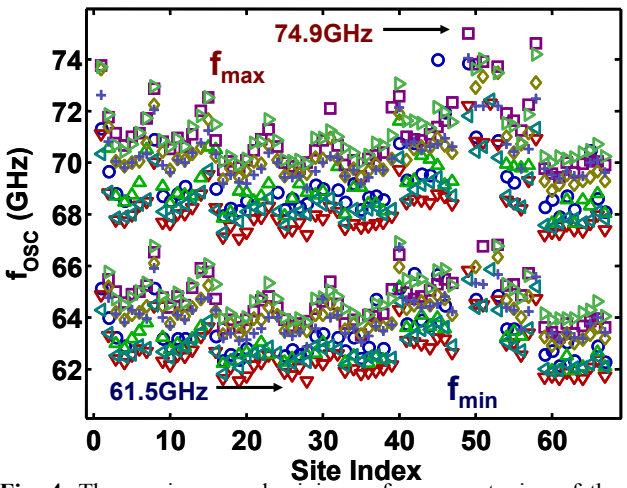

Fig. 4. The maximum and minimum frequency tuning of the LC-VCO. It ranges from 61.5GHz to 74.9GHz. Each marker denotes different wafer. The site index is arbitrary across the wafer.

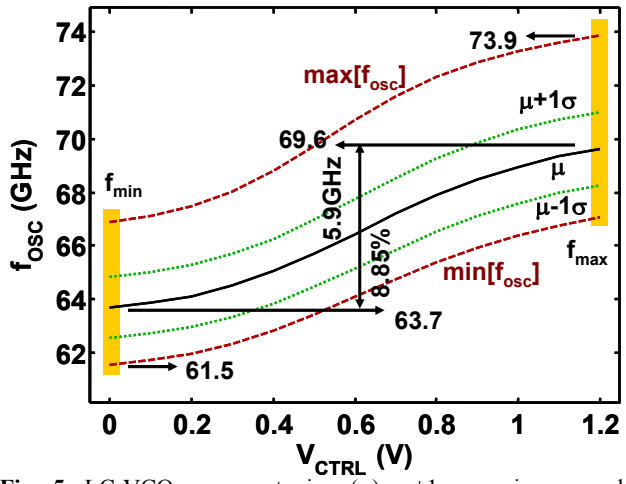

Fig. 5. LC-VCO average tuning (μ), μ±1σ, maximum, and minimum. It shows 5.9GHz and 8.85% FTR. Total 450 VCO data points are used for the statistics.

functions of each other as shown in Fig. 6. Overall, the oscillation frequencies show cross-correlation coefficients ρ greater than 0.66. The FTR is determined by the ratio of tunable varactor capacitance over the total parasitic capacitance. Therefore, the plot suggests that the varactor variation explains significant portion of the LC-VCO frequency variation.

IV. Analog Benchmark for VCO

The VCO data should be examined both from the circuit and technology perspectives for analog benchmark. It advances the conventional digital technology benchmark, so that the analog circuit parameters, CLY, and the CMOS process technology are combined for the product

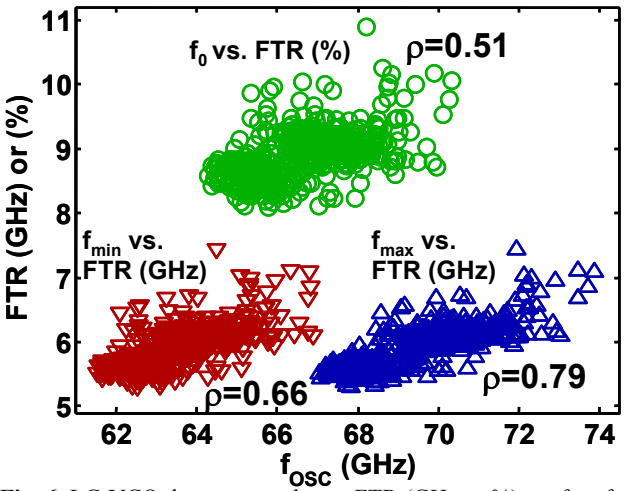

Fig. 6. LC-VCO data scatter plot on FTR (GHz or %) vs. f_{min}, f_0, and f_{max}. The f_{max} shows the cross-correlation coefficient ρ=0.79. It implies that varactor variation plays an important role in the variation.

manufacturability improvement. The VCO data points are used to determine the VCO CLY of a mmWave SoC as plotted in Fig. 7.

The LC-VCO f_{max} and f_{min} show different distributions, where f_{max}'s variation is more stretched. Using the distributions, the yield of the VCO is estimated in Y_{est} for a desired oscillation frequency. The yield from data Y_{data} matches the Y_{est} well. According to the Y_{est}, the VCO will have yield greater than 90% from 65.1 to 67.9GHz. Considering 8.85% FTR, the VCO's FTR is quite wide compared with many of the previously reported mmWave VCOs [5]. In fact, the concern for the yield is more serious than Fig. 7. When a VCO is implemented, there is an offset deviation from the designed center frequency at circuit, wafer, lot level, and so on. The offset decreases the yield further, and the FTR should be even larger.

There are general initiatives to improve the yield: 1) stabilize the analog technology by reducing process variability, 2) design a more manufacturable VCO. Both should be sought simultaneously in practice. The conventional digital benchmark does not provide meaningful information for the LC-VCO as shown in Fig. 8. The plot shows the relation between a 101-stage digital static logic ring oscillator (RO) and the LC-VCO in same chip site. The front-end-of-line (FEOL) ROs are commonly used for digital technology monitoring [6]. The RO is testable at the first metal level, so that only FEOL process modulates the RO performance, though they could be tested at a higher metal level. An assumption here is the proximity and uniformity between the RO and the LC-VCO in a chip site. In the plot, there is not much cross correlation between the two oscillators in both lot and wafer-level data. Also a data set from each wafer makes a

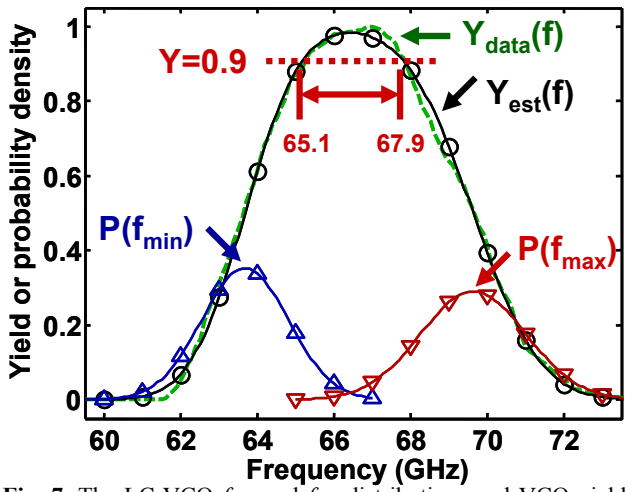

Fig. 7. The LC-VCO f_{max} and f_{min} distributions and VCO yield from data and fitting. The yield fitting Y_{est} is obtained from the f_{max} and f_{min} distributions. The VCO shows 90% yield from 65.1 to 67.9GHz range.

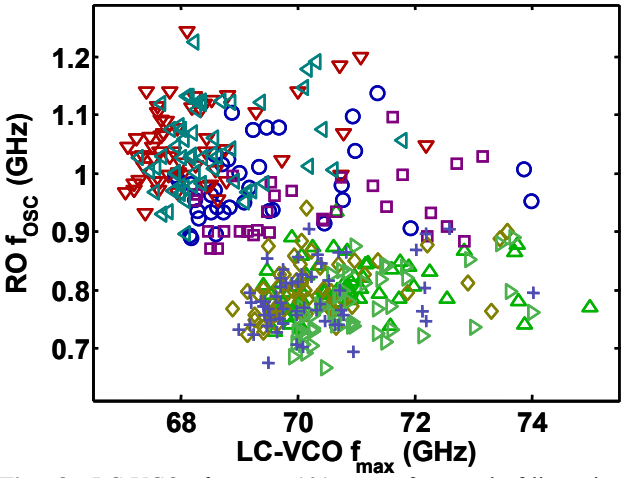

Fig. 8. LC-VCO f_{max} vs. 101-stage front-end-of-line ring oscillator frequency scatter plot. Each wafer has different marker shapes. There are not much statistical relations between the digital benchmark and the LC-VCO f_{max}.

cluster, and the cluster discontinuity among them is not explained by the RO and the VCO. The plot shows that the conventional digital benchmark vehicle is not appropriate for analog circuits. A separate set of analog benchmark structures are necessary with parameters derived from analog and mmWave perspectives.

One of the trends in the process variability in sub-100nm CMOS is the increasing within-wafer, or chip site-to-site variation [2]. It has been observed in digital process monitoring. A similar phenomenon is observed in the analog process variability in Fig. 9. The first iteration of the principal component analysis [7] is used to visualize the variability. The VCO data is filtered to 27 chips and 8 wafers for this analysis, since the analysis requires regular matrix-like data formation. The principal components (PCs) are extracted in wafer and chip site directions by calculating the covariance matrices in wafer and site directions. During the PC extraction, each PC's strength is also obtained as an eigenvalue. The amplitude of each dominant PC is plotted in Fig. 9. The wafer direction PC amplitude is 2.01, and the site direction amplitude is 24.5. The process-induced variability model is essential for circuit design and CMOS process development. The model is useful for variation-resistant circuit design, simulations, and yield estimation. Also the model is used to reduce the variability in the technology development.

VII. Conclusion

The process variability of a V-band LC-VCO fabricated in 65nm SOI CMOS was examined. On average, the VCO tunes from 63.7 to 69.6GHz with 8.85% frequency tuning range. The nanometer CMOS variability deteriorates the chip-limited yield of a mmWave communications system. The circuit design and the CMOS technology development should collaborate to design more robust circuits and to benchmark the analog active and passive device variability.

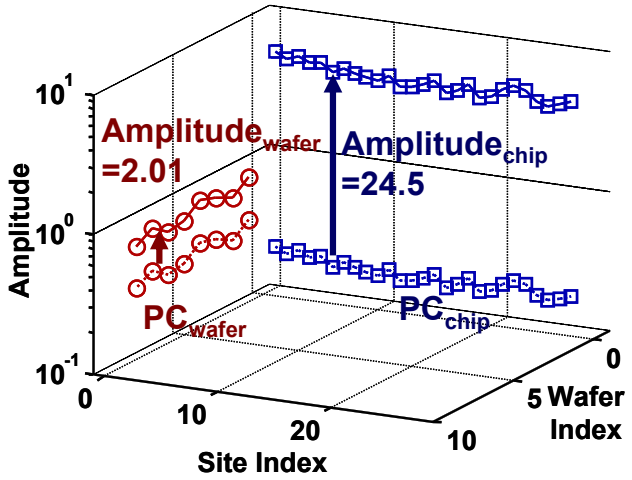

Fig. 9. The dominant principal components and amplitudes in wafer and site variation directions. Total 27 sites per wafer and 8 wafers are used for the calculation.

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