16.3 An Array of 4 Complementary LC-VCOs with 51.4% W-Band Coverage in 32nm SOI CMOS

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CMOS VCOs have been implemented for mm-wave applications [1-7], however, as the required channel bandwidth for these applications increases, wide-range VCO tuning is becoming more challenging. Even without taking into account the process variability in nanometer CMOS, a single VCO hardly achieves requirements for a mm-wave band and phase-noise performance, and it suffers from the steep VCO loop gain. Taking advantage of parallelism, using an array of VCOs is emerging as an alternative technique to implement a wide-band VCO (Fig. 16.3.1). While nanometer CMOS technology is becoming the next generation RF and mm-wave platform (because of high-speed performance due to technology scaling and and SoC integration capability), costly technology developments and mask sets further promote the use of array-based VCOs to expedite yield learning and circuit-development cycle. However, a VCO array requires more circuit area. Conventional designs are not scalable because of their size, cost, and complications for signal delivery. Technology scaling for mm-wave SoC is driven by the high-speed device performance while digital systems benefit from increased device density. In mm-wave applications, passive components, especially inductors, are responsible for area budget, since their area is not scaled with the technology. Taking advantage of nanometer FETs, the presented complementary LC-VCO is attractive for VCO arrays. It uses an LC-tank and its area is minimal and highly scalable. The use of state-of-the-art nanometer CMOS technology is essential to retain high-speed design margin for mm-wave circuits and provisions are required to make the complementary LC-VCO more scalable and manufacturable against the process variability and technology uncertainty. After all, the VCO array provides mm-wave-component performance-variability metrics as a feedback to the technology foundry. Such components are difficult and expensive to characterize and the required on-chip probe pads waste silicon area.

To achieve higher oscillation frequency, multiple-harmonic VCOs have been implemented, but they lack active components that can operate as fast as the VCO itself to implement a practical transceiver system. The fundamental oscillation and mm-wave component implementation capabilities in each technology are constrained by FET transconductance g_m and parasitic capacitances, although circuit-design techniques and technologies are being developed for better performance optimization. The complementary LC-VCO design, shown in Fig. 16.3.1, is presented in this work. The cross-coupled inverter topology allows more balanced and symmetric VCO output swing to improve phase-noise performance and power consumption. It also shows symmetric varactor and VCO tuning with the varactor biasing. By having both NFET and PFET at the output nodes, the VCO is penalized since the PFET has lower negative g_m and higher parasitic capacitance due to $W_{PFET}/W_{NFET} > 1$. Because of the parasitic penalty, the topology serves as benchmark metric that reveals technology performance as a pessimistic bound. SOI CMOS technology has been useful to implement high-frequency VCOs with a wide-tuning capability, taking advantage of the lower source/drain parasitic capacitances of SOI transistors.

The negative-g_m pair is implemented with double-pitch relaxed cell-based FETs with intensive dual-gate contacts and M1 padding across the gate. The M1 wiring is necessary to lower the effective resistance of the intrinsic FET gate, as shown in Fig. 16.3.1. Relaxed pitch enhances FET stress liner efficiency and reduces source- and drain-to-gate parasitic capacitances. An accumulation-mode FET with thick-oxide option is utilized for varactor. It lowers leakage current through the gate oxide, and it reduces body and diffusion resistance for improved Q-factor. First, a varactor cell is optimized for the best Q-factor by changing the gate length. Then, the cell is duplicated in an array to achieve the designed varactor capacitance. Inductor width and length are designed to attain Q-factor for oscillation condition and capacitance contribution to the LC tank. The inductor uses M6 to M10 metal layers populated with vias along the trace. Back-end-of-line fills and patterns modulate the layout, but the overall inductor parameter is estimated and calibrated with EM simulations. The target tuning range is 85 to 105GHz, and 32nm SOI target model parameters are used to estimate and align the VCOs.

The implemented VCOs tune from 83.20 to 96.98GHz (VCO1, 2, and 3) and 100.07 to 104.28GHz (VCO4), and their measurement results are shown in Fig. 16.3.2. Four VCOs cover 51.4% of W-Band (75 to 110GHz), and they can be selectively switched to the desired band. The fastest VCO shows 4.13% frequency tuning from its center frequency of 102.18GHz, as shown in Fig. 16.3.2. As shown in the graph on the right side of Fig. 16.3.5, the VCO extends the frequency tuning range (FTR) versus oscillation frequency boundary among reported state-of-the-art VCOs. The VCO achieves almost 2× frequency tuning range as compared to that of reported above-100GHz VCOs [2,4]. When 880 VCO arrays in 11-wafers from the same batch are tested, they show an average of 49.7% W-Band coverage with 3.21% standard variation as plotted in Fig. 16.3.5. The output power is –30.65dBm at 104.2GHz, after the W-Band mixer corrections. The losses in the cable, adapter, and probe make it difficult to measure phase noise due to the instrument noise floor. By using a W-Band amplifier and optimizing its gain, the signal power is boosted until noise added by the amplifier overwhelms the instrument noise floor. Figure 16.3.3 shows VCO spectrum centered at each oscillation frequency and free-running phase-noise measurements with an amplifier.

Using the inductor and varactor design parameters, the parasitic capacitances experienced by the VCOs are calculated by solving an overdetermined system of linear equations in Fig. 16.3.4. The constant α is the varactor ratio between VCO1 and VCO2, and β is the inductor ratio between VCO1 and VCO3. Unknowns are: varactor minimum capacitance C_0, varactor tunable capacitance ΔC, FET and wiring parasitic capacitance C_{par}, and inductor capacitance C_{ind}. From solving the equations, it turns out that the inductor contributes most to the capacitance, followed by the FET and wiring parasitics. The analysis is useful to monitor technology and device information at mm-wave frequencies. When the method is applied to statistical measurements, the solutions reveal the process variability of the parasitic components in detail. The plot on the right side of Fig. 16.3.4 shows relative capacitance component distribution from 880 chips in a lot of 11 wafers.

In Figure 16.3.6, the performance of the VCO array is compared with that of the state-of-the-art W-Band VCOs. The VCO4 shows a phase noise of –100.9dBc/Hz at 10MHz offset from 104.2GHz. The core draws 6.33mA from a 1.2V supply, or equivalently, it consumes 7.59mW. The VCO FOM is –172.28dBc/Hz and the $FOM_{T=10\%}$ is –164.59dBc/Hz. The VCO occupies $40\times35\mu m^2$, as shown in die micrograph of VCO4 in Fig. 16.3.7. The VCO achieves the widest frequency tuning range among above-100GHz VCOs with the smallest design footprint, low-power consumption, and phase-noise performance suitable for communication SoCs. Note that the 32nm SOI CMOS technology provides a performance gain and has potential application for mm-wave SoC platforms.

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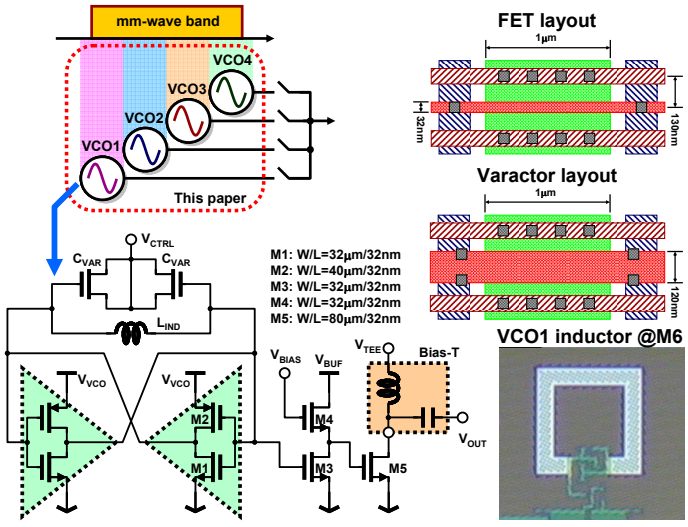
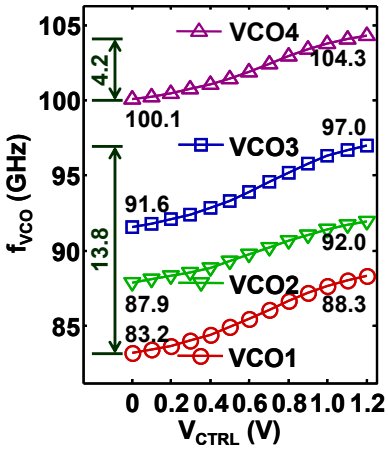


Figure 16.3.1: An array of VCOs for wideband applications and the schematic of the complementary LC-VCO.



	VCO1	VCO2	VCO3	VCO4
Inductor L(μm)×W(μm)	90×5	90×5	80×5	80×5
Varactor W(μm)×L(μm)	70 ×0.12	50 ×0.12	70 ×0.12	50 ×0.12
f_{min} (GHz)	83.20	87.89	91.57	100.07
f_{max} (GHz)	88.29	91.97	96.98	104.28
f_0 (GHz)	85.75	89.93	94.27	102.18
FTR (GHz)	5.09	4.08	5.42	4.22
$K_{v,min}$ (GHz/V)	2.21	1.77	2.27	1.77
$K_{v,max}$ (GHz/V)	5.98	4.87	6.43	5.01
I_{VCO} (mA)	6.07	6.58	6.42	6.31

Figure 16.3.2: VCO tuning range, design parameters, and performance summary.

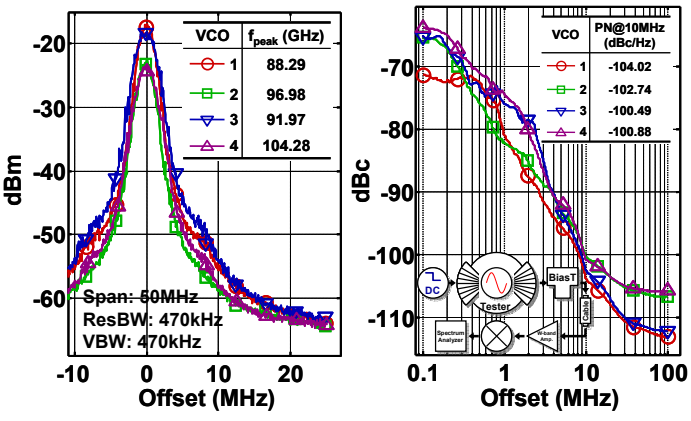


Figure 16.3.3: VCO spectra and phase-noise measurements with a W-Band amplifier.

VCO oscillation frequency

$$f_{vk} = \frac{1}{2\pi\sqrt{L(C_0 + \Delta C_{var} + C_{par} + C_{ind})}}$$

LC-tank design parameters

$$\alpha = \frac{C_{var,VCO1}}{C_{var,VCO2}} \qquad \beta = \frac{L_{VCO1}}{L_{VCO3}}$$

Linear equations

$$\begin{bmatrix} 1/f^2_{v4,min} \\ 1/f^2_{v4,max} \\ 1/f^2_{v3,min} \\ 1/f^2_{v3,max} \\ 1/f^2_{v2,min} \\ 1/f^2_{v2,max} \\ 1/f^2_{v1,min} \\ 1/f^2_{v1,max} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ \alpha & \alpha & 1 & 1 \\ \alpha & 0 & 1 & 1 \\ \beta & \beta & \beta & \beta^2 \\ \beta & 0 & \beta & \beta^2 \\ \alpha\beta & \alpha\beta & \beta & \beta^2 \\ \alpha\beta & 0 & \beta & \beta^2 \end{bmatrix} \times \begin{bmatrix} C_0 \\ \Delta C_{var} \\ C_{par} \\ C_{ind} \end{bmatrix}$$

Component	Ratio (%)
C_0	21.4
ΔC_{var}	9.2
C_{par}	23.8
C_{ind}	45.6

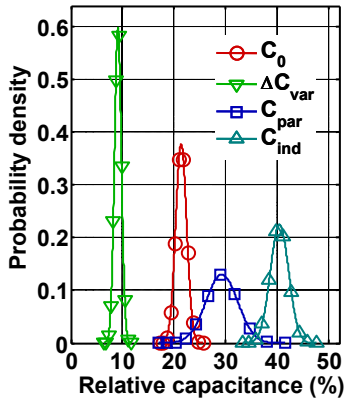


Figure 16.3.4: Capacitance analysis and distribution from 880 chips.

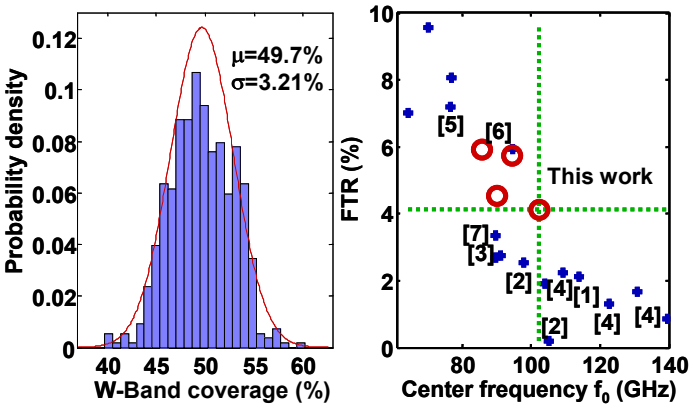


Figure 16.3.5: W-Band coverage statistics and tuning range comparison.

Ref	f_0 (GHz)	FTR (%)	Phase noise (dBc/Hz @ MHz)	P_{DISS} (mW)	FOM (dBc/Hz)	FOMT (dBc/Hz)	VCO core area (μm²)	Technology
[1]	114.0	2.11%	-107.6 @10	8.4	-179.50	-165.96	100800	130nm CMOS
[2]	98.0	2.55%	-102.7 @10	7.0	-174.07	-162.21	72000	130nm CMOS
[2]	105.2	0.19%	-97.5 @ 10	7.2	-169.37	-134.95	72000	130nm CMOS
[3]	91.3	2.74%	-107.1 @ 10	14.0	-174.84	-163.60	272800	90nm CMOS
[4]	109.2	2.24%	-105.2 @ 10	9.6	-176.14	-163.16	48600	90nm CMOS
[4]	122.8	1.30%	-100.2 @ 10	9.6	-172.16	-154.46	48600	90nm CMOS
[4]	139.6	0.86%	-93 @ 10	9.6	-166.07	-144.76	48600	90nm CMOS
[5]	76.6	7.18%	-110.6 @ 10	13.6	-176.95	-174.08	10000	90nm CMOS
[6]	94.6	5.92%	-106 @ 10	9.0	-175.98	-171.42	45050	65nm CMOS
[7]	89.8	3.34%	-95 @ 1	na	na	na	na	65nm CMOS
VCO1	85.7	5.94%	-104.02 @ 10	7.3	-174.32	-169.79	1400	32nm SOI
VCO2	89.9	4.54%	-102.74 @ 10	7.9	-173.04	-166.17	1400	32nm SOI
VCO3	94.3	5.74%	-100.49 @ 10	7.7	-171.36	-166.53	1400	32nm SOI
VCO4	102.2	4.12%	-100.88 @ 10	7.6	-172.45	-164.75	1400	32nm SOI

Figure 16.3.6: State-of-the-art 100GHz VCOs performance comparison.

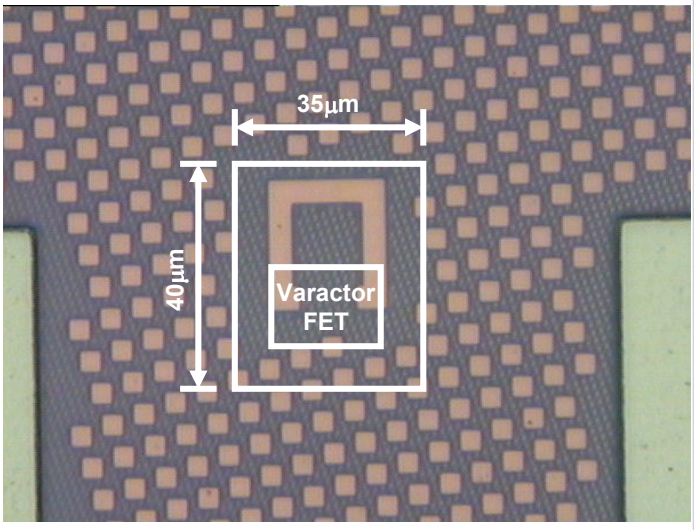


Figure 16.3.7: Chip micrograph of VCO4 at M10.

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