25.5 A 94GHz Locking Hysteresis-Assisted and Tunable CML Static Divider in 65nm SOI CMOS

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As an essential clock-system component, millimeter-wave dividers have been implemented for V- and W-band channels [1-8]. This has also served as a standard benchmark vehicle that reveals high-speed and low-power performances of a technology. Through technology scaling, CMOS CML static divider high-frequency performances have been scaled [6-8], and they are comparable to dividers in other technologies [1-5]. In addition to the device performance, circuit design and measurement determine the divider high-speed and wide frequency range performance. One of the uncertainties in CML static divider measurement is pulling and locking hysteresis. By using CML static divider topology, the divider has been assumed to have a fixed wide operation range, from DC to the $f_{div,max}$, the maximum input-referred divider operational frequency. In fact, the CML static dividers show a certain degree of locking hysteresis, similar to injection-locking dividers [9]. When the circuit sensitivity curve is measured, it is not clear where to set the threshold. Depending on the method, a sensitivity curve can be optimistic or pessimistic. A similar problem lies in the $f_{div,max}$, since it changes depending on the status of a divider. Also, there have not been any analytic results that can interpret the circuit parameters and performance, in spite of the common use of sensitivity curve in literatures.

The CML static divider schematic is shown in Fig. 25.5.1. It has CML-based master-slave FF latches, with AC-coupled RF input and separate DC bias input. To maximize the divider performance, a cell-based FET layout is used with pitch relaxation. It effectively improves the device g_m by enhancing the stress liner efficiency through the opening. The FET parasitic capacitance is reduced due to the increased gate-to-contact spacing. By its nature, the divider exhibits highly nonlinear behavior. It has multiplication as a single-balanced mixer, and the circuit behaviors are quite different in self-oscillation and input-locked modes. An approximate and linearized circuit analysis is used to obtain sensitivity curve and locking hysteresis models. The approximation begins from the tail current i_T modulation by input v_I, and the resulting differential-pair $g_{M,D}$ changes. By assuming that the input is much smaller than the bias tail current I_T, the modulated differential pair $g_{M,D}$ is derived with power series expansion and high-order term omission. The mixing is approximated by ignoring high-frequency terms with an assumption that they are low-pass filtered by the circuit [8]. The result will be more relevant to the high-frequency part of the divider operation due to the assumption. Another assumption is that the circuit is bistable between self-oscillation and input-locked modes. A steady-state circuit equation is established by assuming 270° phase between differential-pair input and output node v_O. In the absence of input signal v_I, the self-oscillation condition and frequency are obtained. The loading capacitance is modeled as C_L. The current sum at the output node v_O is arranged in real and imaginary terms, and the Pythagorean trigonometric identity leads to a divider input-locking condition as an equation of a circle in admittance Y plane.

The implications of the divider locking-condition equation are described in Fig. 25.5.2. Two cases – A) self-oscillation and B) input-locked modes – are plotted on the Y=G+jB plane, where real axis is conductance G, and imaginary axis is susceptance B. The dotted line is the bias line of the differential-pair $G_{M,D}$ and negative g_m pair $G_{M,N}$, and it is assumed to follow a straight line with an angle φ, especially when the tail device sizes are the same. First, at the self oscillation in case A, the bias point moves along the bias line, controlled by DC tail input voltage. On the other hand, for an input-locked mode in case B, the circuit condition moves away from the bias point (the center of the circle) to a point on the circle. The radius of the circle is a function of input signal amplitude A_i. Using the input-locked and self-oscillation models, the CML static divider sensitivity curve and hysteresis effects are obtained, as given in the right plot of Fig. 25.5.2. The obtained hysteresis curves provide predicted hysteresis-assisted amplitude gain and divider operation bandwidth extension $\Delta f_{hys,in}$. The f_{in} is input-referred and the f_{out} is output frequency, and f_{in}=2×f_{out}.

The divider has hysteresis both for amplitude and frequency sweeps according to the proposed model. The amplitude sweep hysteresis model and simulations are plotted in Fig. 25.5.3. Case A is when the input signal amplitude goes down at a fixed frequency from the input-locked state. The divider remains locked until the r_{dn}, or input amplitude of $A_{i,dn}$. Passing r_{dn}, the divider makes a sudden transition to self-oscillation mode, since there is no solution. The downward amplitude-sweep simulation shows the consistent behavior at $A_{i,dn}$. Case B is when the input amplitude moves up at the same frequency from self-oscillation mode. The input modulates the divider output, and the divider tries to lock by swinging along the bias line from the center bias point, till it reaches the input frequency f_i with $r_{up}(A_{i,up})$. The amplitude upward-sweep simulation is consistent to this locking model. At a given bias, an analytic downward sensitivity curve is obtained as $A_{i,dn}(f_{in})$, by solving the minimum required amplitude for downward locking at each frequency. Using trigonometric relation, the upward sensitivity curve is $A_{i,dn}(f_{in})$/cosφ. The hysteresis-assisted amplitude gain is 1/cosφ. The frequency-sweep hysteresis can be modeled similarly. There are complicated mixings well beyond the equation, but the linear model provides useful qualitative observations. The divider has AC-coupled RF input with DC-bias control. Vertical native capacitors are used for AC coupling. The separate DC-bias control tunes divider operating conditions, so that the effective dividable frequency range is widely tuned as shown in Fig. 25.5.4.

The sensitivity curves of the fabricated CML static divider in 65nm SOI are measured as shown in Fig. 25.5.5. The maximum divider operational frequency is 94.446GHz with 64.9mW/FF and 86fJ power-delay product per gate at V_{DD}=2.4V and V_{BIAS}=2.4V. For each V_{DD} and V_{BIAS} setting, the upward and downward input power thresholds between self-oscillation and input-locked modes are measured. At V_{DD}=1.5V and V_{BIAS}=0.5V, the measured hysteresis-assisted gain is 0.74dB. The predicted hysteresis gain is 2.55dB, with the circuit design parameter k=0.894. The minimum power-delay product per gate of 24fJ is recorded at 82.3GHz, when V_{DD}=1.5V and V_{BIAS}=0.5V. Due to the W-band setup limitation, the lower-frequency sensitivity curve is not measured. The circuit still shows true static divider-like wide frequency range from the self-oscillation at 64.7GHz to 82.4GHz. The presented work is compared with state-of-the-art dividers in Fig. 25.5.6. The divider reaches up to 94.4GHz as a true CML static-like wide frequency range divider in CMOS, and the 24fJ power-product delay is the minimum among the dividers above 40GHz with 100×40μm² circuit area.

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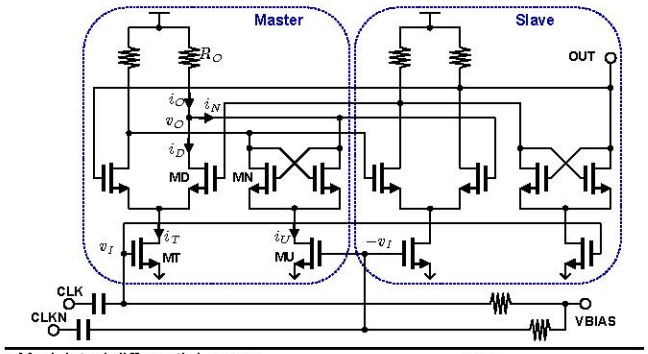


• Modulated differential $g_{M,D}$

$$g_{M,D} \approx \sqrt{\beta_D I_T}\left[1+\frac{i_t(t)}{2I_T}\right]$$

• Self-oscillation frequency

$$f_{SO,out} = \frac{G_{M,D}}{2\pi C_L}$$

• Divider locking condition

$$\left(G_{M,N}-\frac{1}{R_O}\right)^2+\left(G_{M,D}-2\pi f_{out}C_L\right)^2=\left[\sqrt{\beta_D\beta_T+\beta_N\beta_U}\frac{A_i}{2\sqrt{2}}\right]^2$$

Figure 25.5.1: CML static divider schematics and approximate solution.

$$k=\tan\varphi=\frac{G_{M,N}}{G_{M,D}}$$

$$r(A_i)=\frac{\sqrt{\beta_D\beta_T+\beta_N\beta_U}}{2\sqrt{2}}A_i$$

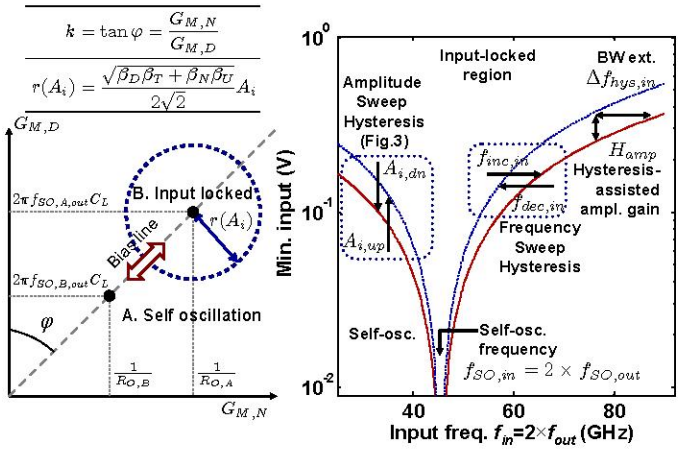


Figure 25.5.2: Divider self-oscillation and input-locked mode diagram.

• Ampl. downward sweep sensitivity curve

$$A_{i,dn}(f_{in}) \geq \frac{2\sqrt{2}}{\sqrt{\beta_D\beta_T+\beta_N\beta_U}}\left|G_{M,D}-\pi f_{in}C_L\right|$$

•Hysteresis-assisted amplitude gain

$$H_{amp}=\frac{1}{\cos\varphi}=\frac{A_{i,up}}{A_{i,dn}}=\frac{r_{up}}{r_{dn}}$$

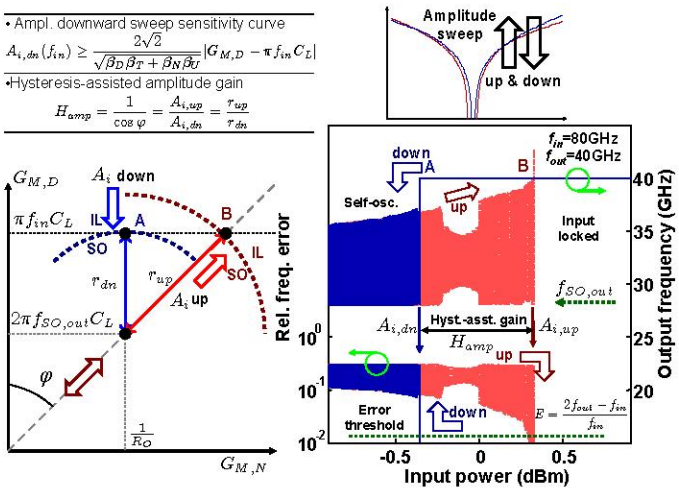


Figure 25.5.3: Divider locking hysteresis during amplitude sweeps.

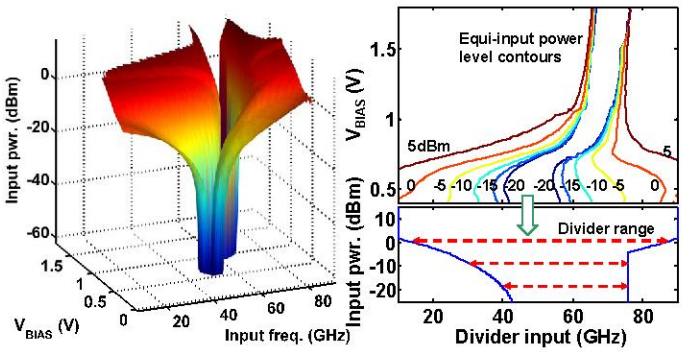


Figure 25.5.4: Simulated divider sensitivity curve and operation tuning.

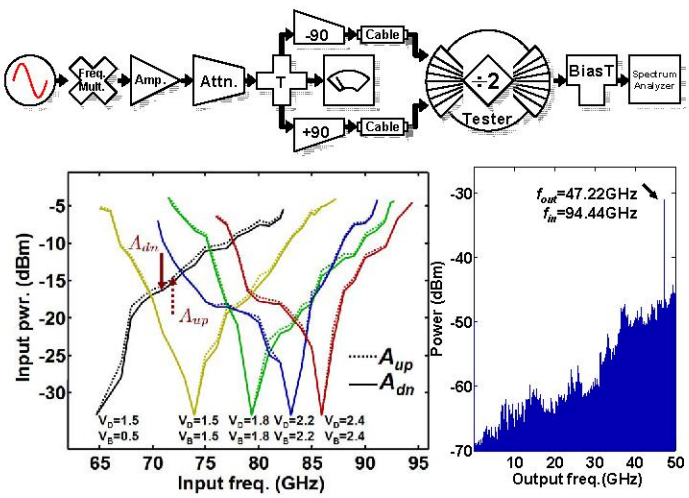
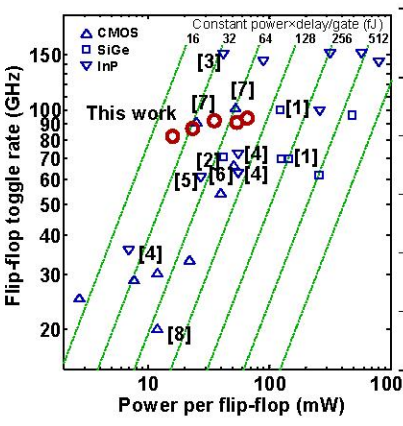


Figure 25.5.5: Test set up, sensitivity measurements, and output spectrum.



V_{DD}	V_{BIAS}	Power (mW)	f_{SO} (GHz)	Avg. H_{amp} (dB)	$f_{div,max}$ (GHz)
1.5	0.5	15.8	32.3	0.74	82.3
1.5	1.5	23.2	37.0	0.46	87.2
1.8	1.8	35.2	39.7	0.55	92.7
2.2	2.2	53.5	41.5	0.46	91.2
2.4	2.4	64.9	43.0	0.44	94.4

Figure 25.5.6: Measurement summary and performance comparison.

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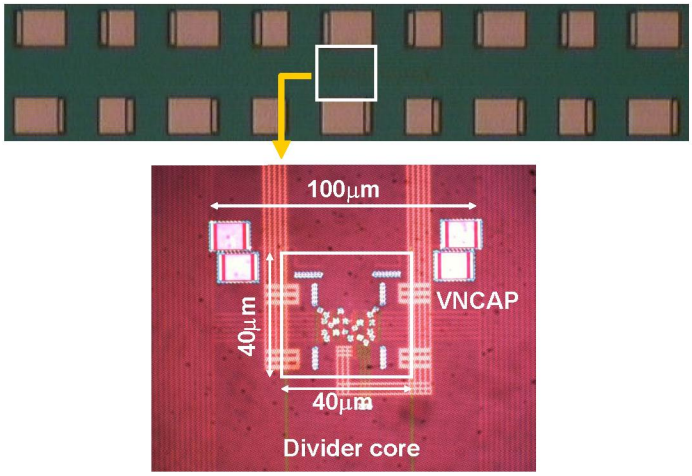

Figure 25.5.7: Chip die micrograph at M10 (top) and M4 (bottom) levels.

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