30.2 A 70GHz Manufacturable Complementary LC-VCO with 6.14GHz Tuning Range in 65nm SOI CMOS

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A complementary LC-VCO is integrated in a 65nm SOI process and is statistically characterized on a 300mm wafer. Average center frequency is 67.9GHz and frequency tuning range is 6.14GHz or 9.05%. It achieves a phase noise of -106dBc/Hz at 10MHz offset and consumes 5.37mW from a 1.2V supply. The VCO yield is 94.7% for 70GHz operation.

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Outline

- Introduction:
  - Motivation
  - Application
- Design discussion:
  - Development platform
  - Design process and components
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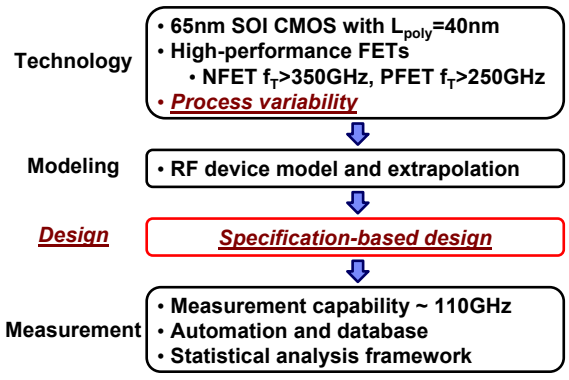
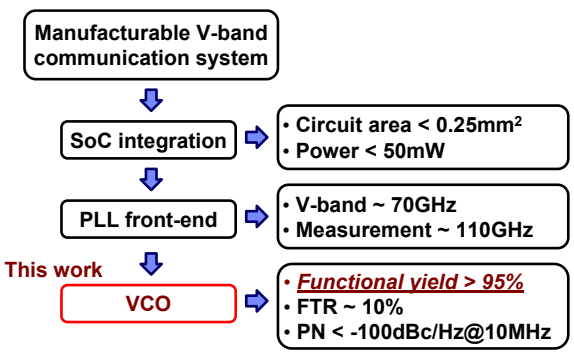
Development Platform



Motivation



Design Concerns

- Oscillation condition

$$g_{m,FET} > k \times g_{m,LC-TANK}, k > 3$$

- Functional yield

$$\text{Yield}(\%) \Leftrightarrow \text{FTR}(\%) \Leftrightarrow \text{CTR}(\%)$$

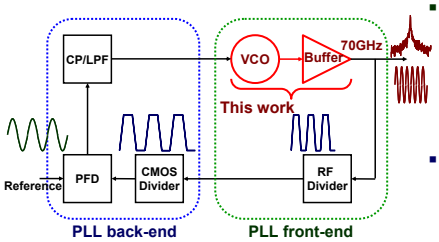
- Phase noise

$$PN = f\left(P_{sig}, Q_{LC-TANK}\right)$$

- Circuit area
- Power consumption

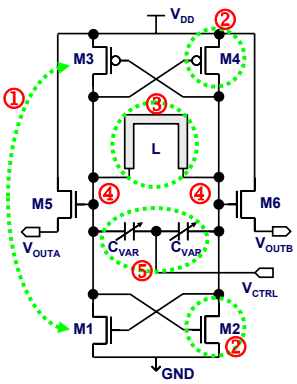
Application

- V-band communication system PLL
  - OC-1536
  - Giga-bit wireless



- PLL front-end
  - High speed
  - Performance
  - Parasitics
  - Variability
- PLL back-end
  - Supportive
  - Lower speed
  - Precision

Schematic Diagram

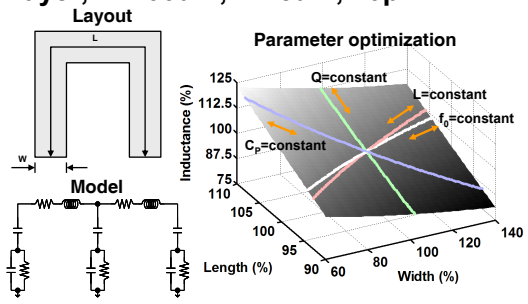


① Symmetry
② FET layout optimization
③ 1.2um-thick Cu top layer
④ Maximum CTR biasing
⑤ Thick-oxide AMOS

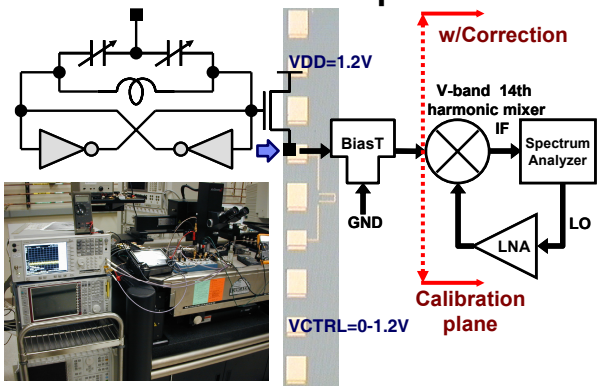
- M1,M2: 14/0.06
- M3,M4: 28/0.06, β=2
- M5,M6: 16/0.06
- CVAR: 68/0.12
- L: 30×40×5
- Parasitics: technology

Inductor

- Microstrip inductor with 1.2um top Cu layer, L=100um, W=5um, 40pH

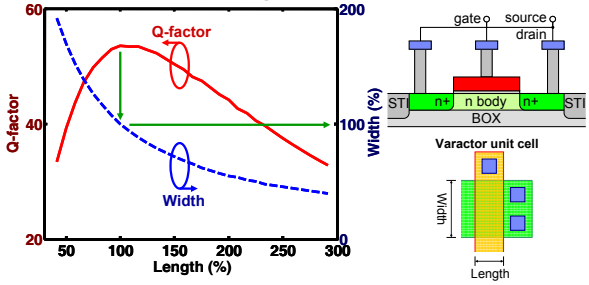


Test Set Up



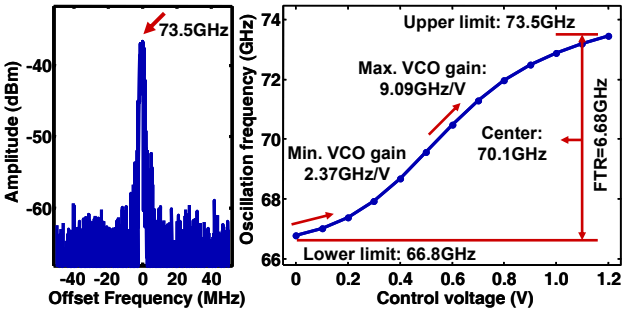
Varactor (AMOS)

- Fixed capacitance and number of cells
- Optimized for highest Q with L & W



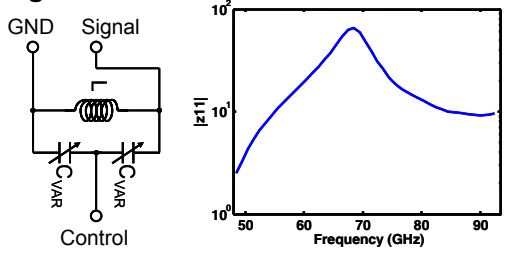
Frequency Tuning Range

- V_{DD}=1.2V, V_{CTRL}=0~1.2V, FTR=9.5%



LC-Tank

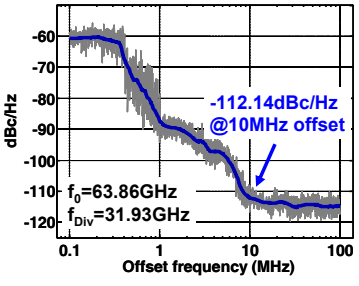
- L & C characterization challenge
- LC-tank VNA measurement
- Single-ended Q=8.5



Phase Noise

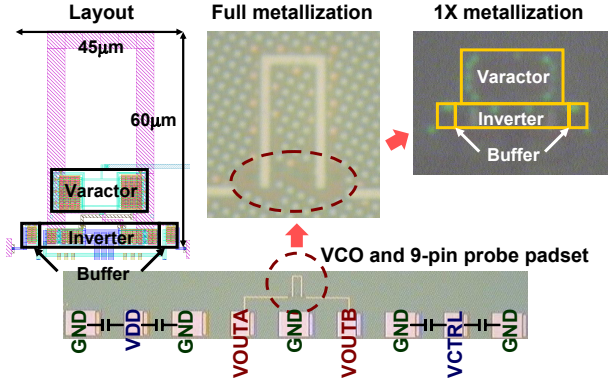
- Measurement with an on-chip divider

$$FOM_T = PN - 20\log\left(\frac{f_0}{\Delta f}\cdot\frac{FTR}{10}\right) + 10\log\left(\frac{P_{DISS}}{1mW}\right)$$



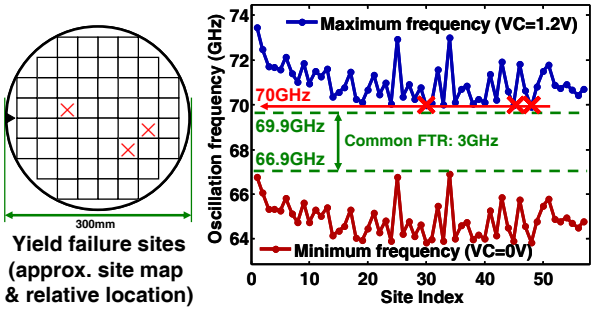
- VCO phase noise = *-106.14dBc/Hz* @10MHz offset
- FOM = -175.8dBc/Hz
- FOM_T = -175.4dBc/Hz

Layout & Die Photo



VCO Functional Yield

- 3GHz common FTR, 94.7% 70GHz yield



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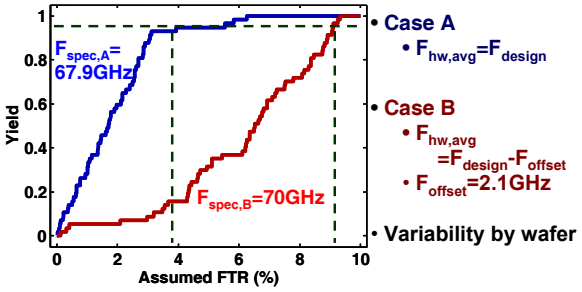
Functional Yield & FTR

- Functional yield is determined by FTR
  - Using measured center frequency data

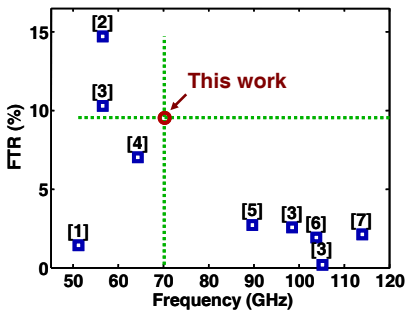


Statistics

	Average	Std. deviation	Norm. dev. (%)	Max.	Min.
Upper limit f_H (GHz)	71.0	0.82	1.15	73.5	69.9
Lower limit f_L (GHz)	64.8	0.76	1.18	66.9	63.8
Center frequency f_0 (GHz)	**67.9**	**0.79**	**1.16**	**70.1**	**66.9**
FTR (GHz)	**6.14**	**0.13**	**2.11**	**6.68**	**5.91**
FTR (%)	**9.05**	**0.17**	**1.90**	**9.53**	**8.72**
Full range VCO gain (GHz/V)	5.11	0.11	2.11	5.57	4.93
Max VCO gain (GHz/V)	7.96	0.43	5.36	9.38	7.25
Min VCO gain (GHz/V)	1.72	0.43	25.0	2.37	0.11
I_{VDD} (mA) @ V_{CTRL}=0	**4.48**	**0.51**	**11.4**	**5.15**	**3.59**

Comparison

- Extends high-yield V-band VCO limits



Conclusion

- A record CMOS VCO with FTR and yield
- Achieved VCO results
  - f_{target}=70GHz with 95% yield
  - FTR_{avg} ~ 9.1%
  - Phase noise ~ -106dBc/Hz @10MHz
  - P_{avg} ~ 5.4mW
  - Circuit area ~ 0.0027mm²=2700μm²
- SOI CMOS is promising for mmWave SoC