Wideband mmWave CML Static Divider in 65nm SOI CMOS Technology

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***Abstract*—A wideband millimeter-wave (mmWave) CML static divider fabricated in 65nm SOI CMOS technology is presented. The mmWave system realization trend and engagement in sub-100nm CMOS technologies are summarized. CML static divider's circuit analysis, sensitivity curve, and simulations are explored. The input-locking hysteresis and divider DC bias tuning are employed to extend the divider operation range. The divider performance measurements are presented with hysteresis-assisted gain and figure-of-merits. A scalable statistical estimation is proposed, and it is validated with a full 300mm wafer measurements. The divider exhibits wideband mmWave performance to overcome the process variability in sub-100nm CMOS processes.**

I. Introduction

The 60GHz range milli-meter wave (mmWave) physical links are emerging as a next generation short-range wide-bandwidth communications channel [1], [2]. The CMOS technology is becoming a strong candidate for the mmWave system design platform due to its manufacturing capability, system-on-chip (SoC) integration with baseband and digital intellectual property, and high-speed performance through technology scaling [3]. As CMOS FET's gate length scales aggressively, the device density has increased, and high-speed performance also has been improved down to 45nm. For example, 45nm SOI NFET's f_T is beyond 400GHz [4], and it provides enough design margin for mmWave analog system, though the device speed will reach the physical limit soon [5]. The adversaries of sub-100nm CMOS are the up-front costs for development and mask [6], and the aggravated defects and process variability [7], [8]. The variability affects the analog clock generation and transceiver front-ends of mmWave SoC more than the digital block. It is because of the small device dimension and parasitic capacitance contribution, which is relative to the total parasitic allowance. Especially the mmWave tranceiver and PLL shown in Fig. 1 are susceptible to the variation. The PLL front-end components - VCO and the pre-scaling frequency divider [9] - are potential bottlenecks for SoC chip-limited yield (CLY) due to the variability. It is essential to have a wideband tunable VCO and wideband divider to overcome the variation, while the technology stabilization is enforced.

This paper presents wideband CML static divider analysis, design, and measurements in 65nm SOI CMOS, as summarized in Fig. 1. The mmWave system implementation trend and the technology-to-circuit interaction between CMOS and mmWave analog system design are discussed as backgrounds in II. The CML static divider design process is reviewed in III. The divider small-signal analysis, sensitivity curve, models for hysteresis between input-locked and self-oscillation modes, circuit design parameters, and simulation results are explored. In IV, divider test methodology is presented. The mmWave test setup, divider measurements, performance comparison, figure-of-merits (FoMs), process variation, and scalable statistical estimation are examined.

II. Backgrounds

The mmWave channel realization trends are reviewed from technology and application perspectives in II-A. The increasing overlap and collaboration between CMOS technology and mmWave analog design are discussed in II-B.

A. Application

The high-definition multimedia contents are overloading existing channels with data bandwidth and the cumbersome cable connections. To meet the demands, the interests on mmWave system have been elevated for last several years [1], [10]–[12]. A survey on IEEE International Solid-State Circuits

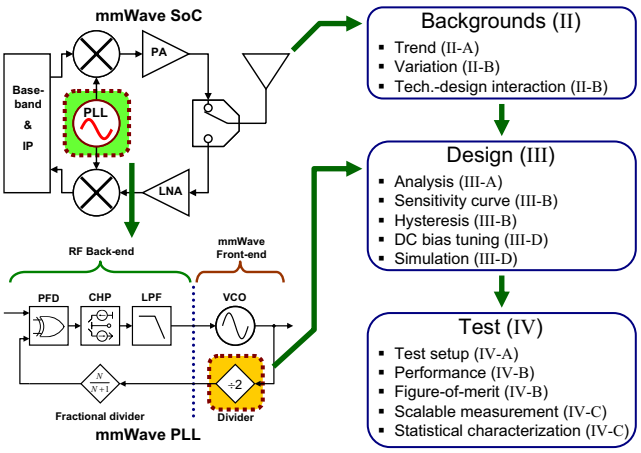

Fig. 1. Overview of the paper. The mmWave channel SoC implementation trend and CMOS technology-to-design interaction are reviewed (II). The PLL front-end frequency divider is the main concern in the paper, and it is susceptible to the process variability in sub-100nm along the VCO. The divider design (III) and measurements (IV) are presented.

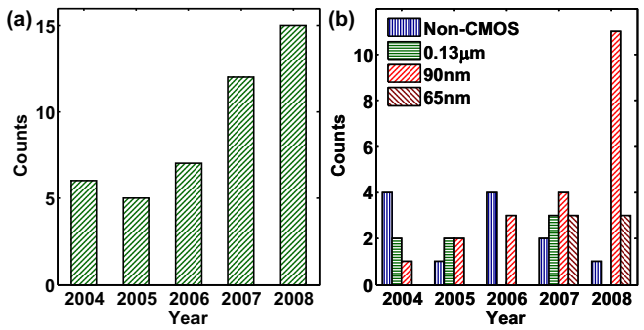

Fig. 2. Last 5-year trend of above-50GHz circuits in ISSCC. (a) The number of papers have been increasing steadily. Also more mature systems and higher-level of integrations have appeared. (b) Technology engagement trend. The 90nm CMOS has become the major platform in 2008, and 65nm implementations begin to appear. There are a few 0.25μm and 45nm entries not shown in the plot for simplicity.

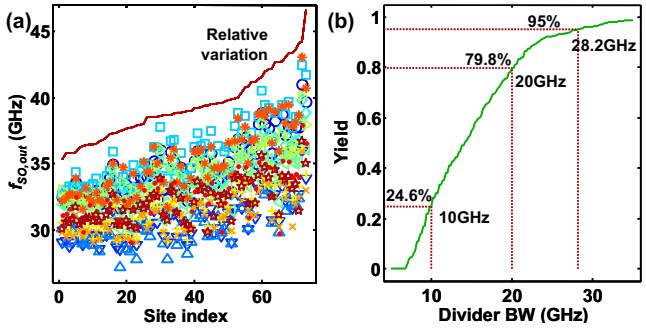

Fig. 3. Divider variability and yield. (a) Divider self-oscillation frequency f_{SO} sorted with the ascending site variation. High-speed circuits involve more variation. The relative variation has no unit and it is scaled to fit the plot. There are 73 site $\times$ 12 wafers = 876 data points. (b) Estimated divider yield with input-referred divider operation bandwidth. A divider meets the specification when it covers at 57-64GHz with a given bandwidth. The bandwidth is assumed symmetric around the self-oscillation frequency. About 28.2GHz operating range is required for 95% yield.

TABLE I
CMOS MMWAVE DIVIDER PERFORMANCE

Type	f_{min}	f_{max}	BW (GHz)	CMOS	Ref.
Static	<64.7	94.4	>29.7	65nm	[17]
	73	100	27	65nm	[18]
	5	66	61	90nm	[19]
Dynamic	85.2	96.2	11	90nm	[13]
	82	94.1	12.1	65nm	[14]
	64	70	6	0.13μm	[15]
	62.9	71.6	8.7	90nm	[16]

Conference (ISSCC) for the last 5 years is given in Fig. 2. Circuits that operates above 50GHz are collected for the plot. The number of papers has increased in Fig. 2(a). In 2008, most of circuits are being implemented in 90nm CMOS, and the number has been increasing steadily. Also 65nm circuits are emerging, beginning in 2007. Once 0.13μm CMOS was considered enough for mmWave, but designers are moving to new scaled technologies for better performance. There are trade-offs among the fabrication cost, foundry access, and the design margin. It is yet to say that 90nm will be the main mmWave platform. It is likely that the popularity will shift toward 65nm and 45nm for the high-speed design margin and state-of-the-art performance.

As shown in Fig. 1, the prescaling frequency divider is an essential function block for mmWave signal generation. Many of mmWave PLL implementations use dynamic injection-locked designs to take advantage of the high-speed performance [13]–[16]. The CML-based static dividers operate at lower frequency, but they have wider operation range [17]–[19]. The dynamic and static classification is based on its operational concept and origin. Their performances are arranged in the Table I. The performances in the table are not necessarily accurate metrics, due to the uncertainties in the measurement setup. Still they are regarded as the best-effort results and demonstration. In general, the CML static dividers offer wider bandwidth than dynamic dividers. Also the CML dividers have reached higher $f_{max,div}$, but the different CMOS technologies make it difficult to compare.

When a mmWave system engages sub-100nm CMOS, the process variability should be considered for manufacturability. The variability of a CML divider is plotted in Fig. 3. One lot of 12 wafers in 65nm SOI CMOS was measured for the plot. It is using self-oscillation frequency f_{SO} to estimated the divider variability [18]–[20]. The variability experienced by injection-locked and CML static dividers is different. Nevertheless, the front-end of line (FEOL) component variation should be similar in both designs. Using the f_{SO} data and divider bandwidth, a CLY of a 57-64GHz mmWave PLL is calculated. In Fig. 3, 28.2GHz divider range is necessary to meet 95% divider yield. Most of dynamic dividers fall short of the bandwidth, and the CML static divider becomes an attractive alternative to overcome the process variation.

B. CMOS Technology and mmWave Design

As mmWave system designs adopt sub-100nm CMOS, the interaction between circuit and device technology becomes essential [21]. The technology complexity, process variability, and system integration challenge should be conveyed to designers. For example, a mmWave designer should be aware of not only technology native device offerings but also secondary options. Fig. 4 shows 65nm SOI CMOS FEOL and back-end of line (BEOL) stack diagram, and device options to make the most out of it. The analog FET performance is optimized with the adjusted gate-to-contact pitches and the number of contacts, as shown in Fig. 4(c). The pitch relaxation improves FET high-speed performance by reducing parasitic gate-to-contact capacitance and enhancing the stress liner efficiency and the carrier mobility [22], [23]. For passives, the technology options should be considered carefully. The different BEOL dielectric materials and air gap [24] could be offered as layer options. Inductor and BEOL vertical native capacitor (VNCAP) designs are determined along the

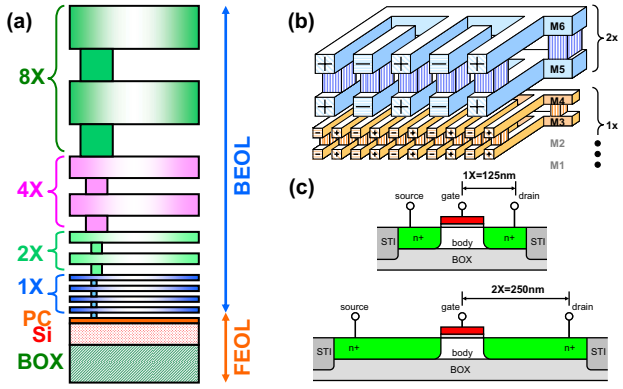

Fig. 4. Analog circuit design requires more knowledge on technology offering with scaling. (a) SOI CMOS technology vertical stack with FEOL and BEOL diagram. (b) BEOL vertical native capacitor (VNCAP) diagram with 1× and 2× metal levels are shown. VNCAP is formed without additional mask sets and scaled with technology. (c) A 65nm SOI NFET diagram with native 125μm pitch between source/drain contacts to poly-Si gate. Also relaxed 2× (250μm) pitch is shown.

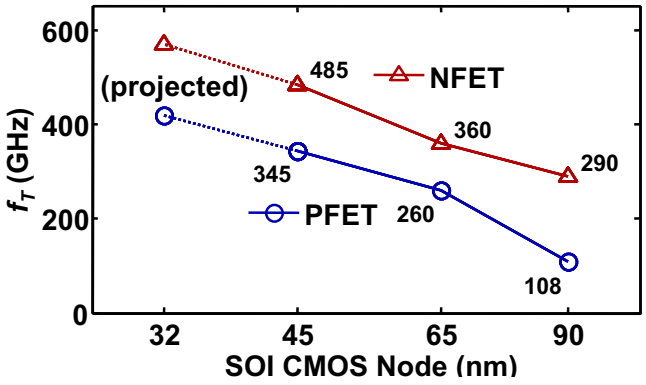

Fig. 5. The SOI CMOS technology current gain cut-off frequency f_T scaling trends in sub-100nm nodes. Not only the device density, but also high-speed performances have been scaled down to 45nm node.

technology options [25], [26]. After all, the CMOS platform itself becomes a menu to choose. CMOS performance has been scaled in high-speed performance so far as shown in Fig. 5 [4], [22], [27]. High-speed analog device performance will be improved along the novel digital device development, such as asymmetric FET and FinFET, and node scaling. The technology adoption trend in Fig. 2 shows that 90nm becomes the majority for mmWave circuits. Previously, 0.18 and 0.13μm CMOS technologies have been RF SoC design platform for several years. The mmWave CMOS platform adoption is limited by the technology accessibility, process variability, model uncertainty, manufacturing stability, and development and mask costs. It will take years to complete the technology performance exploration and mmWave system integration.

III. CML Static Divider Design

The CML static divider design process is described. The circuit is analyzed with small-signal model in III-A. The analytic results are used to derive sensitivity curve and hysteresis models in III-B. The circuit design is reviewed in III-C. The analysis is supported by circuit simulations in III-D.

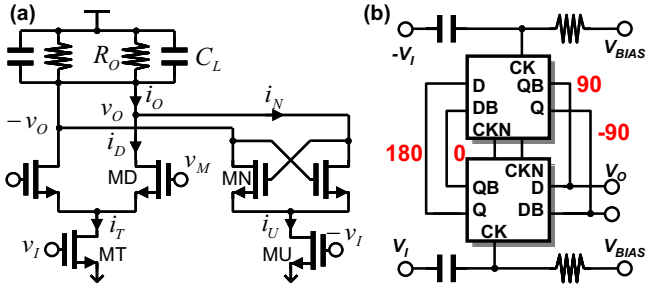

Fig. 6. CML static divider schematic diagrams. (a) A latch stage with a differential and a negative g_m pairs. (b) Divider as a master-slave flip-flop with AC coupled RF input and DC bias V_{BIAS} control. The phase relation is used to model the divider in steady state.

A. Circuit Analysis

CML static divider topology is analyzed with a small-signal model and approximations. Fig. 6 shows diagrams of a latch stage and a divider as a master-slave flip-flop. The topology and its variants have been implemented in several CMOS generations [17]–[19], [28], [29] and non-CMOS technologies [30], [31]. They are referred to as static dividers, in contrast to the dynamic injection-locked dividers [13]–[16]. The topology also has been implemented as technology performance benchmark vehicles. In spite of the common use, the circuit has not been analyzed in detail. The use of sensitivity curve for performance characterization lacks a general model, whereas VCO has phase noise models [32].

The CML static divider is solved by approximating the differential stages as single-balanced mixer and with steady-state complex analysis at the output frequency. The circuit small-signal analysis is based on several assumptions. They are: 1) Small-signal approximation of differential pair g_m, 2) Input and output frequency locking in single-balanced mixer, 3) Steady-state operation at output frequency, and 4) Bi-stable divider status between input-locked (IL) mode and self-oscillation (SO) mode.

The differential pair small-signal gain $g_{M,D}$ is modulated by the tail input v_I and tail current, and it is approximated with a power series expansion assuming that tail DC current is much larger than small-signal current $i_t \ll I_T$. Then high-order terms are ignored.

$$g_{M,D} \approx \sqrt{\beta_D I_T}\left[1 + \frac{i_t(t)}{2I_T}\right] \tag{1}$$

The differential pair output current $i_D = g_{M,D} \cdot v_m$.

$$i_D(t) = G_{M,D} v_m(t) + \sqrt{\frac{\beta_D \beta_T}{2}} v_i(t) v_m(t) \tag{2}$$

The multiplication term $v_i(t)v_m(t)$ involves complicated harmonics as a mixer. For simplicity, the input v_i frequency f_{in} is twice of local v_m frequency f_{out}. The third harmonic at $3f_{out}$

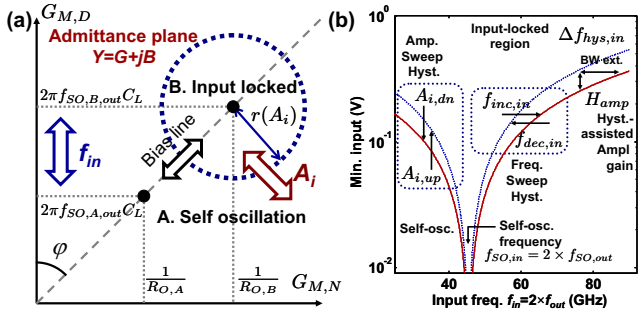

Fig. 7. CML static divider small-signal solution diagram. The approximations lead to an admittance plane circle or point equation. (a) Small-signal SO and IL modes diagram. The divider remains at the bias line for SO. For IL mode, the circuit condition deviates from the bias line to lock the divider to the input signal. The small-signal circuit solution stays on a circle, whose radius is a function of input signal amplitude A_i. (b) Input-referred frequency sensitivity curve with hysteresis. The small-signal solution suggests that there will be hysteresis in amplitude and frequency directions.

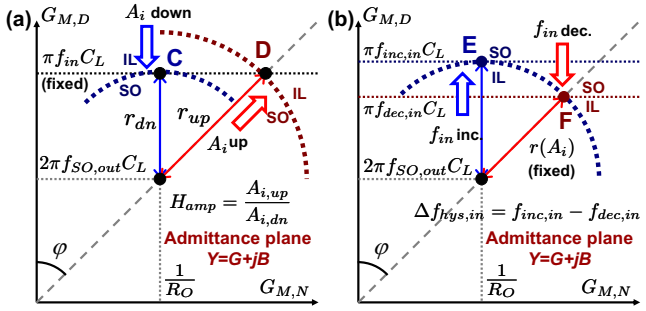

Fig. 8. CML static divider amplitude and frequency hysteresis models. (a) Amplitude sweep hysteresis model. The input signal amplitude A_i's downward sweep from IL mode experiences a step transition at point C to SO mode with a frequency jump. The A_i's upward sweep begins to lock when the self-oscillation frequency meets the desired output frequency at point D. (b) Frequency sweep hysteresis model. The input frequency f_{in} increase from IL mode sweep makes a frequency jump at point E to SO. The f_{in} decrease sweep locks to input when f_{SO} reaches the desired output frequency at F.

is ignored. It is because the entire loop works as a low-pass filter at high-frequency region [28].

$$v_i(t)v_m(t) \approx \frac{A_i A_o}{2}\cos\left[2\pi f_o t + \frac{\pi}{2} + \phi\right] \tag{3}$$

At the output frequency, the circuit node maintains steady-state phase noted in Fig. 6(b), including inversion from differential stage. The local input v_M and output v_O in Fig. 6(a) has 90-degree difference. The ϕ is the phase difference between RF input v_I and output v_O. The $-v_I$ in Fig. 6(a) has a 180-degree phase difference at the input frequency. The steady-state current summation at the output node is in (4). The R_O and C_L are the effective small-signal load resistance and capacitance at the output node. The equation is solved in real and imaginary terms, using trigonometric relations and the Pythagorean identity. Then it is arranged as an equation of circle in (5), for geometric visualization and analysis. The $G_{M,N}$ and $G_{M,D}$ are considered as both variables and constants. It denotes a circle on admittance plane $Y = G+jB$. It is centered at $(1/R_O, 2\pi f_{SO}C_L)$, where f_{SO} is the self-oscillation frequency. The radius is a linear function of input signal amplitude A_i. Considering angles θ and ϕ, not every point on the circle is a solution for the circuit, but it is useful for the circuit behavior visualization.

B. Sensitivity and Hysteresis

The analytic results are utilized to develop divider sensitivity curve and hysteresis models. The implications of the circle in (5) is explained in Fig. 7. There are two cases: A) self-oscillation (SO) and B) input-locked (IL) modes. We assume that the divider is bistable between the SO and IL modes. When $A_i = 0$, the radius of the circle is 0, and the solution remains on the bias line as a point. This corresponds to the SO mode. In the IL mode, input should be strong enough $A_i > 0$, so that the circuit solution moves away from the bias point to a point on the circle. By adjusting V_{BIAS}, the bias point moves along the bias line. For given a condition, a divider in IL mode will exit the mode and enters SO mode, when either input frequency or A_i changes so that IL mode solution does not exist. Also a divider in SO mode will remain in the same mode, moving along the bias line until it finds an IL mode solution. Using the model, the divider sensitivity curve and hysteresis model in Fig. 7(b) are obtained.

The derivation begins with amplitude direction hysteresis at a fixed frequency in Fig. 8(a). When the divider input amplitude A_i goes down from an IL mode, there is more than one solution until point C. Passing C, the divider will make a step-like frequency transition to SO mode, since there is no solution for IL mode. When A_i goes up from a SO mode, the output frequency moves along the bias line till it meets the desired output frequency at D. The divider moves into the IL mode smoothly, by moving along the circle.

The definition of the divider sensitivity curve (SC) is the minimum input power that a divider operates at each frequency. Therefore, there are two different minimum power levels, whether it begins from IL or SO mode. The A_i downward sweep SC $A_{i,dn}(f)$ is more optimistic, and it is obtained by calculating the minimum A_i necessary to remain locked at the desired output and input-referred frequency $f_{in} = 2f_{out}$.

$$A_{i,dn}(f_{in}) \geq \frac{2\sqrt{2}}{\sqrt{\beta_D\beta_T + \beta_N\beta_U}}|G_{M,D} - \pi f_{in}C_L| \tag{6}$$

The A_i upward sweep SC is $A_{i,up} = A_{i,dn}/\cos\varphi$, using the trigonometric relation in Fig. 8(a). The curves in Fig. 7(b) are obtained with (6) and scaling by $1/\cos\varphi$. The SC slope is $2\sqrt{2}\cdot\pi C_L/\sqrt{\beta_D\beta_T + \beta_N\beta_U}$ (V/Hz), and it serves as a FoM. Fig. 8(a) predicts the frequency-direction hysteresis, whose model is described in Fig. 8(b). For frequency sweep, the A_i, or the radius of the circle is fixed. When input frequency increases from IL mode, there is more than one solution till point E. After E, the divider will make a sudden frequency change to SO mode, since there is no solution beyond E. As the input frequency decreases from SO mode, there is no solution on the bias line, until it reaches point F. Then the divider will be able to lock to input gradually without frequency change.

$$-\left[\frac{1}{R_O}+j2\pi f_o C_L\right]=-jG_{M,D}-G_{M,N}+\left[j\sqrt{\frac{\beta_D\beta_T}{2}}+\sqrt{\frac{\beta_N\beta_U}{2}}\right]\frac{A_i}{2}e^{j\phi} \tag{4}$$

$$\left(G_{M,N}-\frac{1}{R_O}\right)^2+\left(G_{M,D}-2\pi f_o C_L\right)^2=\left[\frac{A_i}{2\sqrt{2}}\sqrt{\frac{\beta_D\beta_T}{2}+\frac{\beta_N\beta_U}{2}}\right]^2 \tag{5}$$

C. Circuit Design

The CML divider was implemented in 65nm SOI CMOS. The circuit does not have waveguides, and relies on discrete active and passive components. In the early technology development stage, the device and parasitic models are far away from the reality. Though the design uses target models, the divider high-speed performance tends to improve over generation, while the topology ensures wideband operation against process variation. The model f_{SO} is about 40GHz, and the estimated sensitivity curve slope $|\partial A_i(f_{in})/\partial f_{in}|$ is about 11.6mV/GHz. For a 0.5V peak-to-peak input, the divider will operate up to $2\times f_{SO}$+21.6GHz=101.6GHz.

To maximize the divider high-speed performance, relaxed $2\times$ gate-to-contact pitch FETs are used with dual gate connections. The g_m gain from the pitch relaxation is about 6.7%, while the g_{ds} also increases, so that the self gain is reduced. Still the NFET f_T is enhanced by 15.2% [23], and the layout optimization is useful to boost the circuit design margin. The pitch relaxation does increase circuit area by about 41%, but it is still small compared with passive components and interconnects. The FET sizes are W_D=10 and W_N=8μm, and the differential pair must be stronger than the negative g_m pair to overwrite latch.

A poly resistor of about 200Ω is used instead of a PFET load to reduce the output node v_O parasitic loading. An inductive load can be used to cancel out capacitance [18], [33], and to improve high-speed performance, which would increase circuit footprint. The BEOL VNCAP was used for AC coupling [25], [26]. The VNCAP implementation is highly compatible with digital CMOS technology, and requires no additional mask sets. Also capacitance density and qualify factor is comparable to MIM capacitors. To reduce substrate coupling, the lowest metal layer was avoided. It reduces the capacitance density, but the Q-factor should be higher slightly. The Q-factor is limited by the minimum feature metal layers ($1\times$) due to line resistance, and twice width ($2\times$) metal staggered capacitance has lower metal resistance. The VNCAP area is $10\times10\mu$m^2, and estimated capacitance is about 200fF. The VNCAPs were also used to decouple the power supply connections around the circuit. For testing, a pair of 150μm-pitch RF+DC wedge probe padsets were placed in the layout. The divider core area is about $40\times40\mu$m^2.

D. Simulation

Differential signals are directly applied to the tail gate without AC coupling and resistor. Signal DC level is used as V_{BIAS}. The output is terminated with a bias-tee so that

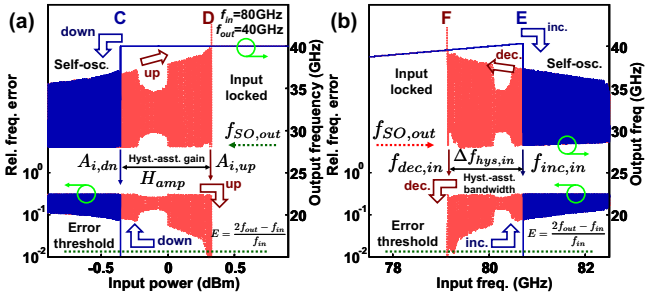

Fig. 9. CML static divider hysteresis simulation. (a) Amplitude sweep hysteresis simulation. At 80GHz, input signal amplitude is swept between IL and SO modes. The upper curves show the divider output frequency and the lower curves are relative frequency error. The divider is in IL mode when the error is below a preset 1% threshold level. As predicted in the model, the A_i-downward sweep makes a step-like frequency transition at C, while upward sweep smoothly moves to IL mode from SO at D. (b) Frequency sweep hysteresis simulation at 0dBm input power. The frequency-increasing sweep makes a sudden transition at E, as described in the model, and the frequency-decreasing sweep makes a gradual transition at F.

only AC components are visible at the output. After extracting the zero-crossing timing, and comparing the period with input frequency, the divider IL or SO mode is determined. Before obtaining divider SC, amplitude and frequency sweep hystereses are observed with in Fig. 9. The error threshold level is 1% of input frequency to determine the divider mode. The amplitude sweep was performed at 80GHz. As modeled in III-A, the input signal amplitude upward $A_{i,up}$ and downward $A_{i,dn}$ sweeps show different threshold levels. The $A_{i,up}$ needs more signal power to lock to input, and $A_{i,dn}$ maintains IL mode for lower input power. The ratio between the $A_{i,up}$ and $A_{i,dn}$ is considered as an amplitude-direction hysteresis gain H_{amp}, so that the divider can operate with lower input level when the initial condition is IL mode. Similar phenomenon is observed with frequency sweep in Fig. 9(b). The frequency operation range is effectively extended by $\Delta f_{hys,in}$, when the frequency and amplitude conditions begin from the IL mode.

As discussed, there are two SCs, one for upward $A_{i,up}$ and the other for downward $A_{i,dn}$ as plotted in Fig. 10(a). The amplitude hysteresis is noticeable at the high frequency, and therefore it extends the divider operation range. As expected, the hysteresis transition depends on the sweep speed, step size, and number of repetition. An example is plotted in Fig. 10(b). In the plot, the upward- and downward- amplitude and the frequency-increasing and decreasing sweeps are overlaid. The hysteresis-assisted operation extension range overlaps, but they are not exactly same. There are simulation errors since the hysteresis behavior is subject to simulation sweep setup. The

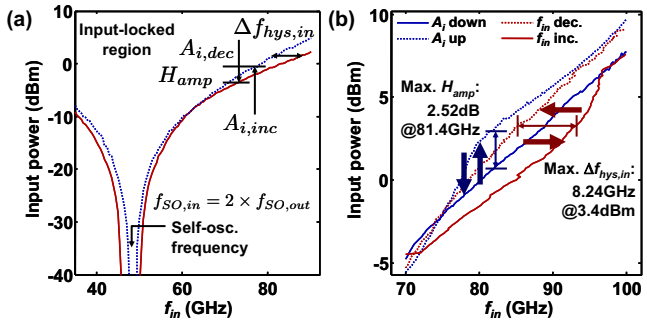

Fig. 10. CML static divider hysteresis simulation results. (a) Amplitude sweep SC and hysteresis over wide input frequency range. (b) A zoomed frequency and amplitude window was repeated with more detailed sweeps in frequency and amplitude. Two hysteresis extension ranges overlap, but they are not exactly same.

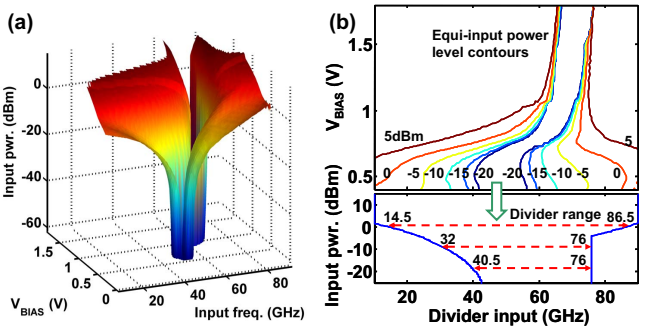

Fig. 11. CML static divider SC tuning with DC bias. (a) 3-D plot with V_{BIAS} tuning. (b) Effective dividable frequency with minimum input power at each frequency.

frequency sweep gain is more important since a VCO makes frequency-direction sweeps for PLL locking.

Using separate DC tail control, the divider can adjust the f_{SO} and bandwidth. While the operation bandwidth decreases as V_{BIAS} increases, still it is a useful technique to broaden the effective operation range. The V_{BIAS} sweep with $A_{i,dn}$ SC is in Fig. 11. It shows the divider SC in 3-D. By obtaining the minimum input power level that the divider operates at each frequency across V_{BIAS} conditions, an effective operation range is obtained in Fig. 11(b). With V_{BIAS} tuning, the divider can accept low-level power over wide range. For example, it operates from 32 to 76GHz, or a 44GHz bandwidth at -10dBm power level.

IV. Measurements

The divider measurements, variation, and statistical scalable characterization are discussed. The test setup is introduced in IV-A. The divider performances and FoM are compared in IV-B with hysteresis and bias tuning. Divider performance variation, benchmark, and statistical scalable divider characterization are discussed in IV-C.

A. Test Setup

A typical test setup photograph and a diagram are in Fig. 12. The difficulty of mmWave CML divider test originates

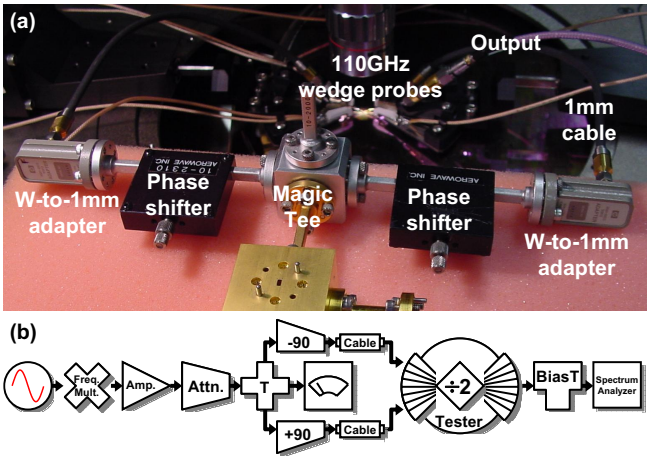

Fig. 12. (a) Divider test setup photo. The W-band waveguide limits below-65GHz low-frequency range access. (b) Test setup diagram. The input signal power is calibrated with a power meter at the magic tee input. Signal loss in the W-band connection makes it difficult to estimate the actual power that reaches the circuit input. Phase shifter needs to be adjusted at each frequency for better divider performance.

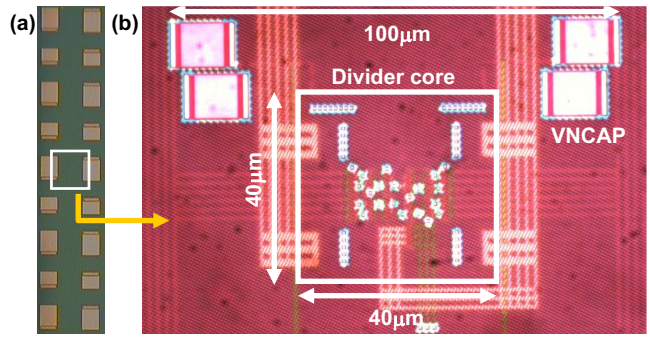

Fig. 13. Divider chip die photos taken at (a) top metal (M10) and (b) fourth metal (M4) levels. Two 150-μm pitch wedge probe padsets are used for RF and DC connections. Small dots are inter-metal vias, and bright squares are BEOL VNCAPs for AC coupling and power supply de-couplings.

from high-frequency input, setup signal loss, and differential input. A 6× frequency multiplier is used to generate W-band frequency, from a 50GHz signal source. It is leveled greater than 10dBm by a W-band amplifier. The signal is attenuated for divider experiment, and it is split into two paths with a magic tee. Phase shifters adjust signal phases to make differential inputs. After exiting waveguides, differential signals go through 1mm cables and 110GHz wedge probes. The input power is calibrated at the output of the attenuator, and it is not trivial to estimate the real power at the circuit input. The setup is not appropriate for frequency sweep SC, since the phase shifter introduces uncertainty.

B. Measurement

The divider was fabricated in 65nm SOI CMOS as shown in the die photograph in Fig. 13. The divider output frequency is captured and compared with the input signal through spectrum analyzer. To determine the divider IL and SO modes

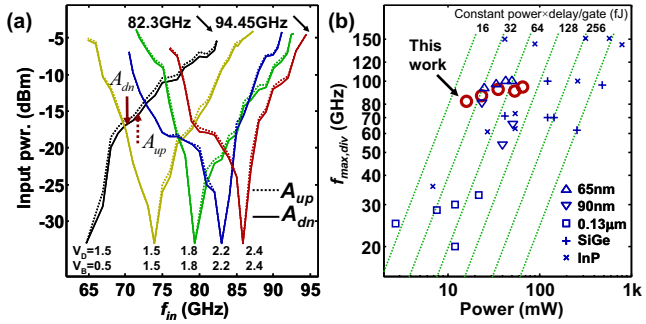

Fig. 14. CML static divider sensitivity curve measurements and FoM. (a) The solid line is a downward and the dotted line is an upward amplitude sweep sensitivity curves. An optimistic 3dB signal loss is assumed from the attenuator to the circuit input. The maximum hysteresis gain observed is about 0.74dB at V_{DD}=1.5 and V_{BIAS}=0.5V. (b) Power-delay product has been used as a divider FoM. The circuit power is normalized by the number of equivalent logic gates. CMOS dividers operate at V- and W-bands with minimal switching energy performances.

TABLE II
CML STATIC DIVIDER PERFORMANCE

V_{DD}	1.5	1.5	1.8	2.2	2.4
V_{BIAS}	0.5	1.5	1.8	2.2	2.4
Power (mW)	15.8	23.2	35.2	53.5	64.9
$f_{SO,out}$ (GHz)	32.3	37.0	39.7	41.5	43.0
Avg. H_{amp} (dB)	0.74	0.46	0.55	0.46	0.44
$f_{div,max}$ (GHz)	82.3	87.2	92.7	91.2	94.4

TABLE III
CML STATIC DIVIDER FOM

Ref.	Tech.	f_{max} (GHz)	$\frac{P}{8f_{max}}$ (pJ)	$\lvert\partial A_i/\partial f\rvert$ (mV/GHz)	$\Delta f/f_{SO}$ ratio
[31]	InP	143.6	78.3	79.8	1.392
[34]	SiGe	72.8	94.4	91.7	1.841
[19]	90nm	66.0	96.6	83.3	1.271
[18]	65nm	100.2	63.2	282.0	0.256
This	65nm	82.3	24.0	85.0	0.545
work	65nm	94.4	85.9	282.6	0.215

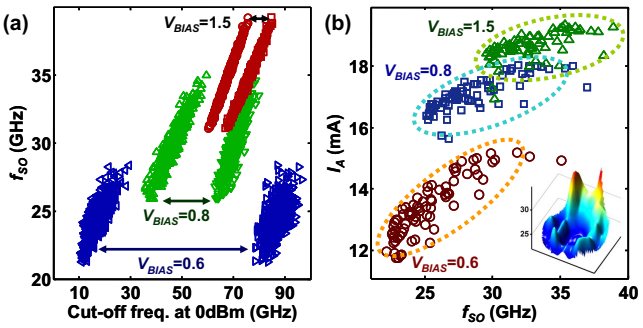

Fig. 15. Divider statistical simulation and measurement. (a) Simulation of divider cut-off frequency at 0dBm with different V_{BIAS}. Total 500 Monte Carlo points are used. The f_{in} increase and decrease sweeps are simulated, and the output is analyzed to obtain at which frequency a divider switches to SO from IL mode. There are strong correlations between f_{SO} and cut-off frequencies. (b) Divider active current I_A and f_{SO} at several V_{BIAS} settings. They show good correlations. The data were obtained from 73 chip sites in a 300mm 65nm SOI wafer, whose mappping is at the bottom right.

accurately, the phase noise of input and output should be compared. In practice, the spectral purity of the divider is observed. Three upward and downward amplitude sweeps are measured and averaged at each frequency, and the upward and downward SCs are plotted in Fig. 14. Several different V_{DD} and V_{BIAS} combinations were used to obtain the plot, and their performances are arranged in Table II. In case of V_{DD}=1.5V and V_{BIAS}=0.5V, the average hysteresis gain H_{amp} between upward and downward SCs is about 0.74dB.

The divider performance comparison has been done with the maximum divider operation frequency $f_{max,div}$, divider bandwidth, and the power-delay product [34] in Fig. 14(b). As described in the mmWave test setup, the actual power at the circuit input is not readily available, and it is obtained from test equipment signal loss estimations. The input power level in each paper is different depending on the setup and calibration. Still they are considered as best-effort measurements. Table III shows FoM comparison with f_{max}, power-delay product [34], SC slope (mV/GHz), and bandwidth over f_{SO} ratio [28]. When a divider has wide operation range, the SC slope $|\partial A_i/\partial f|$ tends to have lower value, and the bandwidth to f_{SO} ratio $\Delta f/f_{SO}$ becomes larger. While the table provides perspectives on the design, a new FoM that considers the setup power level uncertainty should be developed.

C. Scalable Statistical Characterization

The sub-100nm CMOS variation is one of the motivations for wideband CML static divider as discussed in II-A and Fig. 3. It is necessary to measure divider variation to estimate yield, while just one SC measurement is time consuming, and its automation is difficult due to the nonlinearity. The (6) states that a SC is defined when we have circuit design and DC parameters, and f_{SO} as a RF parameter. Therefore, the divider SC performance is reliably estimated with DC measurements and f_{SO}, assuming a good model-to-hardware correlation (MHC). With this estimation method, the statistical characterization of a divider becomes scalable.

The estimation begins with Monte Carlo simulations on the divider bandwidth as plotted in Fig. 15(a) and DC parameters, such as active and quiescent currents I_A and I_Q. The plot suggests that the f_{SO} reflects the frequency direction cut-off frequency well. Also I_A and I_Q are useful to enhance the estimation accuracy. An estimator is trained with the simulated cut-off frequency, I_A, I_Q, and nominal SC. Then hardware results, such as I_A and f_{SO} data in Fig. 15(b), are used to scale and to offset the estimator for MHC. The divider SC estimation from scalable DC and f_{SO} measurements is verified by sampling divider sensitivity thresholds at 65 and 70GHz with 73 dividers in a 300mm wafer as shown in Fig. 16(a).

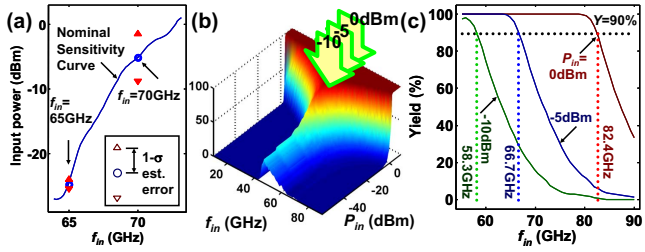

Fig. 16. Divider statistical measurement and estimation. (a) Divider estimation errors at 65 and 70GHz. Overall RMS error is 55% of standard deviation. (b) Divider yield calculation for input power and frequency. Yield is obtained from the scalable statistical measurements. (c) Yield plot slice at 0, -5, -10dBm inputs. The divider operates up to 82.4GHz at 0dBm with 90% yield.

Whole SC curve measurements on all chip sites are too time consuming, and do not add much information. The estimation RMS error is about -2.2dB of 1-σ standard deviation. Using the estimator, the dividers statistical yield for input power and frequency is calculated in Fig. 16(b). For example, the divider will have 90% yield for a 0dBm input at 82.4GHz, as plotted in Fig. 16(c).

V. Conclusion

The wideband CML static divider design and measurements in 65nm SOI CMOS were presented. Circuit analysis provided design equations, evaluation metrics, and scalable statistical method. The wideband divider overcomes the process variability in sub-100nm CMOS technology, and therefore useful as a prescaling frequency divider in mmWave PLL front-end. The scalable statistical measurements proved that divider's wideband capability enables high-yield operation.

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