

A GHz-Digital Clock Jitters in Time and Frequency

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Abstract—The GHz-digital clock jitter measurement capabilities in time and frequency domains are explored. A 101-stage inverter-based ring oscillator implemented in 65nm SOI is used as a clock source. Both domains produce clock period jitters reliably. Cycle-to-cycle jitters are obtained in time, and confirmed in frequency domain. Time interval error jitters are calculated from phase noise, and time-domain results are matched with frequency-dependent jitters. The convergence and limitations of time and frequency-domain jitter measurements are presented.

I. INTRODUCTION

The clock speed of microprocessors reaches well beyond GHz range with deep sub-100nm scaling of CMOS technology [1]. As a result, the distinction between digital high-speed (HS) test in time domain and analog radio frequency (RF) measurement in frequency domain becomes less noticeable with respect to the frequency [2], [3], [4], [5], [6]. As the digital clock frequency increases, a HS test requires high-speed instruments with a fast front-end and a deep memory. The RF test methods become an alternative, especially when such instruments are not available, due to technology limitations. In spite of the theoretical time-frequency equivalency, there are many complications when GHz-range time and frequency measurements are performed in practice. In general, digital clocks are implemented with inverter or current-mirror logic-based ring oscillators to have wide tuning range and to ease integration. The ring oscillators tend to have lower equivalent Q-factor [7], and therefore they have worse phase noise and jitter properties than passive resonator oscillators. The on-chip clocks are used not only for logic timing, but also communication between blocks for computational scalability. Consequently, as the digital clock frequency and logic complexity increases, the clock quality becomes a critical challenge for system specifications.

This paper discusses following three types of jitter for a digital system clock [8], [9]:

- Clock period (CP) standard deviation (σ_{CP})
- Cycle-to-cycle (CC) standard deviation (σ_{CC})
- Time interval error (TIE) standard deviation (σ_{TIE})

These jitters are characterized in time and frequency-domain instruments simultaneously to evaluate the measurement capability from each domain. As described in Fig. 1, digital system clock specifications are defined as jitters in time domain and phase noise in frequency domain. When they are measured in the same circuit, they should produce common and compatible

figures. In practice, they need additional analysis and translations. It is because each domain measurement has advantages and disadvantages for the complete specifications. A 1GHz precision ring oscillator (PRO) with a RF output is used as a test vehicle. Jitter measurements in time and frequency domains are compared and the mismatch is evaluated.

II. RADIO FREQUENCY AND HIGH-SPEED TESTS

In this paper, the RF test is concerned with a frequency region that is used for commercial a communications system, and the HS test is more related to the clock speed of a digital computation system. A state-of-the-art microprocessor reaches clock frequency close to 6GHz [1]. As summarized in the Table I, RF signal is used with modulation, and it has concentrated power near a carrier frequency. The HS test treats baseband signal without modulation, and it has white noise-like spectrum. The frequency-domain instrument operates in real-time, but it shows average power spectral density (PSD). Also it has wide dynamic range and noise floor close to physical limits. The time domain instrument samples and stops before the statistical analysis, but it records real events in the time axis. The frequency-domain range is extended by a mixer for higher speed, but the time-domain sampling speed

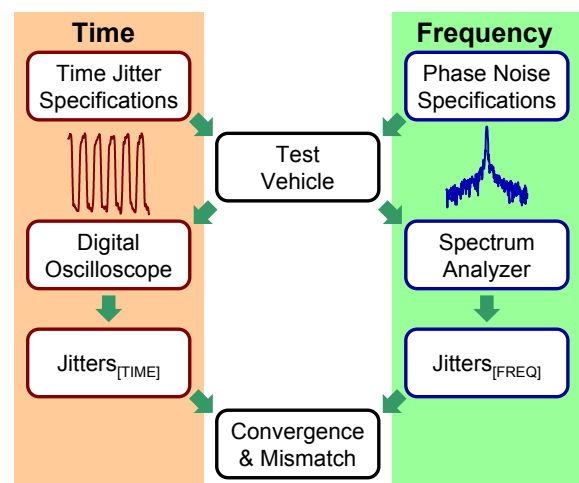


Fig. 1. Clock jitter analysis and convergence process in time and frequency domain. Jitter and phase noise are defined in time and frequency domain respectively. A 1GHz 101-stage precision ring oscillator implemented in 65nm SOI CMOS is used as a test vehicle. Jitter in each domain is compared to demonstrate convergence and limitations.

TABLE I
RADIO FREQUENCY AND HIGH-SPEED SIGNAL AND JITTER
MEASUREMENT

Signal	RF	HS
Generation	modulation	baseband
Bandwidth	near f_O	DC to f_O
Spectrum	strong f_O	white noise
Jitter Spec.	phase noise	statistics
Measurement	Frequency	Time
Dimension	freq. & power	time & amp.
Test speed	real-time	sample and analysis
Representation	average PSD	time waveform
Temporal statistics	n/a	DSP
Sensitivity	noise floor	rough
Dynamic range	high	low
Front-end	mixer, LNA, & ADC	LNA, ADC, & memory
Max. freq.	mixer	LNA and ADC

improvement is not trivial.

Fig. 2a shows a test set up for GHz-digital clock measurements in time and frequency. A digital clock source is a 101-stage inverter-based PRO, implemented in 65nm SOI CMOS technology. A PRO represents the clock source quality available in a technology without using inductors [7]. As depicted in Fig. 2a, the PRO has a RF buffer for precise jitter and phase noise measurements. The instrument outputs are plotted in Fig. 2b. The PRO power supply V_{CTRL} is controlled by a PLL analyzer (Agilent 5052A, left) with a pseudo PLL locking. The PRO phase noise is monitored by a spectrum analyzer (Agilent E4448A, center), and the time jitters are measured through a digital oscilloscope (Tektronix TDS7704B, right), which has 7GHz signal visibility with maximum 20GS/s sampling. The spectrum analyzer and the scope are synchronized through an external trigger source [10]. The jitters are defined in both domains despite of several limitations, as summarized in Table II. The clock period σ_{CP} , cycle-to-cycle σ_{CC} , and time-interval error σ_{TIE} are of interest in this report. Time-domain jitter is estimated after the scope samples waveform for a duration. The same jitters are calculated from the phase noise curve. Other statistics, such as average period μ_p , and peak-to-peak value are only measured in the time domain.

III. JITTERS IN TIME DOMAIN

The scope captures the PRO output waveform for a given duration with a known sampling period. After sequencing, a DSP code performs jitter analysis. It generates a threshold value between the upper and lower peaks, and then estimates the threshold crossing timing τ_k of each clock cycle, as shown in Fig. 3a. The n-th clock period p_n is the time difference $\tau_{n+1} - \tau_n$, as shown in Fig. 3b. Jitters σ_{CP} [5], [3], [4], σ_{CC} [5], and σ_{TIE} [2] are calculated with the equations in Table III. Average clock period is $\mu_P = \lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=1}^N p_n$, and it is approximately same as $\mu_{CP[T]}$. Using definitions, it is shown that $\sigma_{CP} = \kappa \cdot \sigma_{CC}$, and $\kappa = \sqrt{2}$ for an uncorrelated

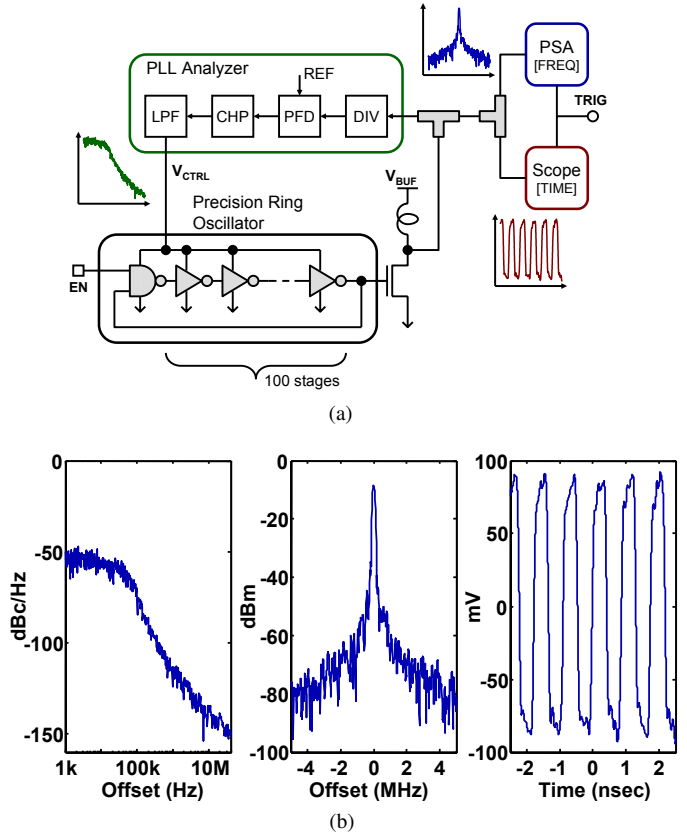


Fig. 2. Time and frequency-domain jitter experiment set up and instrument outputs. (a) The PRO has a RF buffer bias by a bias-tee. The PLL analyzer pseudo-locks the PRO for 1.14GHz oscillation near $V_{CTRL}=1V$. The instruments are triggered for synchronization. (b) The PRO output captured by the PLL analyzer (left), the spectrum analyzer (center), and the digital oscilloscope (right).

TABLE II
JITTER NOTATIONS

Notation		Descriptions
Time	Frequency	
$\sigma_{CP[T]}$	$\sigma_{CP[F]}$	Clock period Std. Dev.
$\sigma_{CC[T]}$	$\sigma_{CC[F]}$	Cycle-to-cycle Std. Dev.
$\sigma_{TIE[T]}$	$\sigma_{TIE[F]}$	Time interval error Std. Dev.
τ_n		n-th clock switch time
μ_p		Average period
p_n		n-th clock period, $\tau_{n+1} - \tau_n$
$MAX + \Delta$		$p_{max} - p_{max-1}$
$MAX - \Delta$		$p_{max} - p_{max+1}$
$L_{[T]}$	$L_{[F]}$	phase noise in dBc/Hz
$LF_{[T]}$	$LF_{[F]}$	phase noise PSD in W/Hz

cycle-to-cycle distribution, and it is up to $\kappa = \sqrt{3}$ from empirical data. The sampling rate should be several times higher than the Nyquist rate to determine the threshold-crossing timing accurately. As plotted in Fig. 3c, the jitter results are compromised when the time resolution and the sampling rate is reduced. This causes a trade-off between the maximum time duration for long-term jitter observation and the TIE

TABLE III
JITTER DEFINITIONS IN TIME AND FREQUENCY

Jitter	Std. Dev.	Mean	Std. Dev. from phase noise
Clock period	$\sigma_{CP[T]} = \lim_{N \rightarrow \infty} \sqrt{\frac{1}{N} \sum_{n=1}^N (p_n - \mu_p)^2}$	$\mu_{CP[T]} = \frac{1}{N} \sum_{n=1}^N p_n$	$\sigma_{CP[F]} = \sqrt{\frac{f^2 \cdot LF(f)}{f_{OSC}^3}}$
Cycle-to-cycle	$\sigma_{CC[T]} = \lim_{N \rightarrow \infty} \sqrt{\frac{1}{N} \sum_{n=1}^{N-1} (p_{n+1} - p_n)^2}$	$\mu_{CC[T]} = \frac{1}{N} \sum_{n=1}^{N-1} (p_{n+1} - p_n)$	$\sigma_{CC[F]} = \kappa \cdot \sqrt{\frac{f^2 \cdot LF(f)}{f_{OSC}^3}}$
Time interval error	$\sigma_{TIE[T]} = \lim_{N \rightarrow \infty} \sqrt{\frac{1}{N} \sum_{n=1}^N (\tau_n - n \cdot \mu_p)^2}$	$\mu_{TIE[T]} = \frac{1}{N} \sum_{n=1}^N (\tau_n - n \cdot \mu_p)$	$\sigma_{TIE[F]} = \frac{\sqrt{2 \cdot \int_0^\infty LF(f) df}}{\omega_{OSC}}$

measurement. As a result, the σ_{TIE} is not estimated accurately due to limited low-frequency jitter information at 20GS/s, or increasing measurement timing error below 20GS/s. The TIE measurement provides SSB phase noise result through a Fourier transform. The accuracy of TIE measurement would be further discussed in time and frequency comparison section V.

IV. JITTERS IN FREQUENCY DOMAIN

The spectrum analyzer shows average PSD of a RF signal. By zooming into near-carrier frequency, single-side band (SSB) phase noise is measured. The unit of the PSD is Watt/Hz, and the phase noise unit is dBc/Hz before the $10 \cdot \log(\cdot)$ [11]. The phase noise becomes a phase noise PSD by removing the $10 \cdot \log(\cdot)$. Using an equivalent noise voltage model [2], the time domain TIE jitter $\sigma_{TIE[T]}$ is equivalent to frequency-domain root-mean squared jitter $\sigma_{TIE[F]}$. The $\sigma_{TIE[F]}$ is obtained from phase noise PSD $LF(f)$ integration, as shown in Table III. An approximate of the integral with the trapezoid rule in (1) is useful for this. In the equation, f_n is an n-th frequency value out of N points, and LF_n is the corresponding SSB phase noise PSD in W/Hz.

$$\int_0^\infty LF(f) df \approx \sum_{n=1}^{N-1} \left[\frac{1}{2} \cdot (f_{n+1} - f_n) \cdot (LF_{n+1} + LF_n) \right] \quad (1)$$

Using $\sigma_{TIE[F]}$ equation in Table III, $LF_{[F]}(f)$ notation in Table II, and (1), the SSB phase noise is converted to time-domain equivalent TIE jitter $\sigma_{TIE[T]}$, as shown in Fig. 4. The lower-frequency phase noise affects the $\sigma_{TIE[F]}$. The first 43kHz of phase noise explains 90% of TIE. Though the SSB phase noise does not have DC to 100Hz, it is relatively a small portion in the total $\sigma_{TIE[F]}$. The $\sigma_{TIE[F]}$ jitter contribution from a specific offset frequency band can be calculated with the similar equations. Also the SSB phase noise provides ways to estimate $\sigma_{CP[F]}$, using equations in Table III, and $\sigma_{CC[F]}$ as long as the κ is known.

V. TIME VS. FREQUENCY DOMAIN JITTERS

As mentioned in section III, the time-domain measurement does not produce accurate $\sigma_{TIE[T]}$ value at 1GHz oscillation

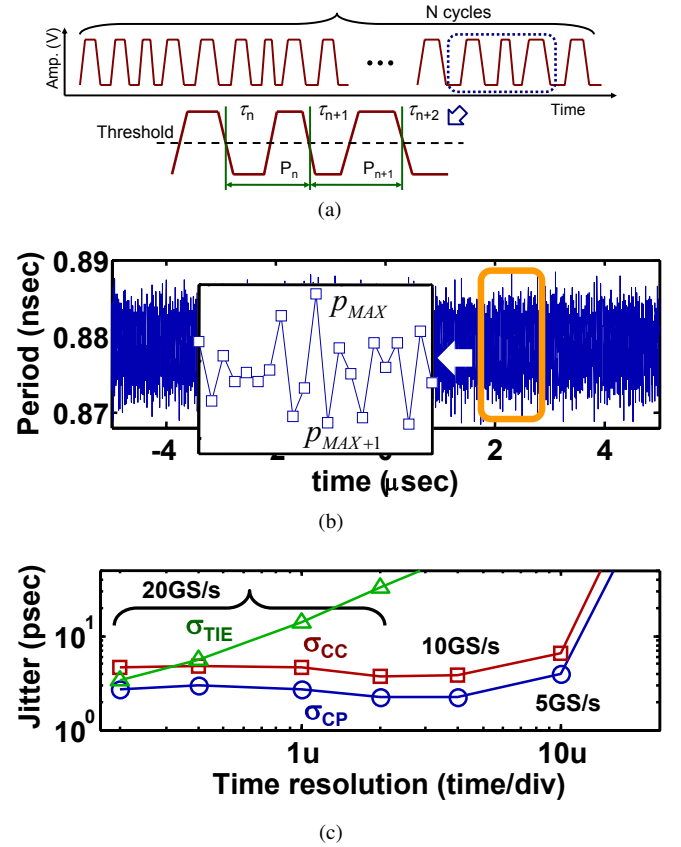


Fig. 3. The PRO time domain jitter measurements with the oscilloscope. (a) The scope sets a threshold value and determines the threshold-crossing timing (τ_n). (b) The obtained time trend of the PRO clock period. Various statistics are derived with the plot. (c) The scope's sampling rate is a critical factor of the measurement accuracy. The jitters are perturbed by threshold timing error below 20GS/s. The σ_{TIE} is limited by both bandwidth and timing resolution

due to limited information on slow-varying jitter and timing inaccuracy. The frequency-dependent jitter components of σ_{TIE} are verified through Fourier transform in Fig. 5. It uses frequency-reversed integral $\bar{\sigma}_{TIE}$ in (2).

$$\bar{\sigma}_{TIE}(x) = \int_x^\infty LF(f) df \quad (2)$$

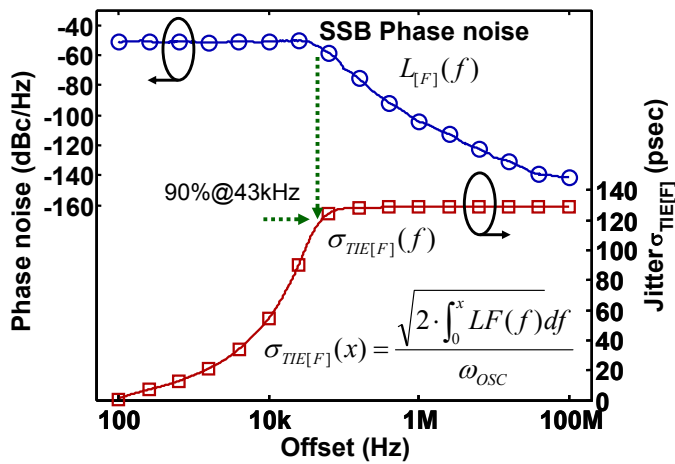


Fig. 4. SSB Phase noise, or phase noise PSD in W/Hz, and accumulated $\sigma_{TIE[F]}$ from 100Hz to offset frequency. Phase noise from 100Hz to 43kHz contributes 90% of $\sigma_{TIE[F]}$.

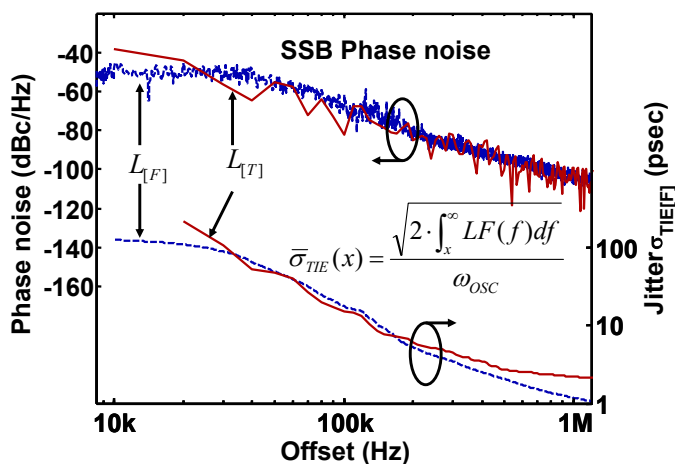


Fig. 5. Phase noise from frequency and time domain, and the frequency-reversed $\bar{\sigma}_{TIE}$ estimation. Both results match from 40kHz to 200kHz range.

Fig. 5 emphasizes the high-frequency compatibility of phase noise L_T and L_F , and their $\bar{\sigma}_{TIE}$'s from 40kHz to 200kHz range. At the low frequency, as the $L_T(f)$ loses spectrum estimation accuracy at 10kHz, the $\bar{\sigma}_{TIE}$ mismatch is maximized. At the high-frequency, the noise floor of the instrument causes deviation. The PRO oscillation frequency is tuned by changing V_{CTRL} from 0.9GHz to 1.1GHz. The σ_{CP} measurements in both domains match within 0.05% error as arranged in Table IV. Since the κ is not obtained in frequency domain, $\sigma_{CC[F]}$ calculation used κ from time domain, which varies from 1.5 to 1.7. As discussed, time-domain $\sigma_{TIE[T]}$ results are not justified without frequency-domain SSB phase noise and $\sigma_{TIE[F]}$. Still the frequency-specific σ_{TIE} from time and frequency domain match well.

VI. CONCLUSION

The time and frequency-domain digital clock jitter measurement capabilities were demonstrated with the 1GHz clock source.

TABLE IV
RF AND HS DIGITAL CLOCK JITTER MEASUREMENTS

Freq.	Domain	σ_{CP}	σ_{CC}	κ	σ_{TIE}
0.9GHz	Time	2.272	3.785	1.666	-
	Freq.	2.271	3.783	-	132.0
	Error	0.03%	0.05%	-	-
1.0GHz	Time	2.209	3.741	1.694	-
	Freq.	2.208	3.739	-	179.0
	Error	0.04%	0.06%	-	-
1.1GHz	Time	3.123	4.670	1.495	-
	Freq.	3.123	4.670	-	145.0
	Error	0.00%	0.00%	-	-

- Time-domain measurement provided jitter statistics including $\sigma_{CP[T]}$, $\sigma_{CC[T]}$, and κ
- Frequency domain RF measurements produced $\sigma_{CP[F]}$, phase noise and $\sigma_{TIE[F]}$
- Both domains showed convergence of σ_{CP}
- Frequency domain needs a time-domain result to calculate $\sigma_{CC[F]}$
- There is limited compatibility with σ_{TIE}
- Both time and frequency-domain measurements are needed to have a complete jitter analysis.

ACKNOWLEDGMENT

The authors would like to thank to IBM engineers R. Trzcinski, K. Rim, G. Patton, and L. Su for their support.

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