In-Situ and At-Speed Modeling and Characterization of Logic Interconnect Device Considering Front-End/Back-End Interaction

Choongyeun Cho, Daeik D. Kim
IBM Semiconductor R&D Center
Hopewell Junction, NY
Email: {cycho,dkim}@us.ibm.com

Jonghae Kim
Qualcomm
San Diego, CA
jonghaek@qualcomm.com

***Abstract*—The paper presents a logic interconnect device (LID) to model digital circuit with near back-end-of-line (BEOL) effect, and to measure system performance. It is driven by a product inverter-based logic circuit, and it is loaded with near-BEOL wiring. The LID ring oscillator is measured and analyzed in 65nm SOI CMOS. The methodology offers in-situ characterization of near-BEOL interconnect parasitics, and dielectric constant in product circuits. It captures front-end-of-line (FEOL) and near-BEOL interactions, distinguished in deeply scaled CMOS.**

I. Introduction

As CMOS technology scales down to sub-100nm nodes, it becomes challenging to maintain digital system performance and yield at the same time. The development effort on the front-end-of-line (FEOL) is diminished by device parasitics, and near back-end-of-line (nBEOL). The nBEOL is defined as the minimum width and pitch metal layers that are immediate to FEOL, i.e. contact, M1, V1, M2, and more, subject to BEOL stack option. The interaction between FEOL and nBEOL is complicated by optical proximity correction (OPC), chemical and mechanical polishing (CMP), lithography-based distortion, and FEOL enhancement techniques, such as spacer and stress liner [1], [2]. The scaling worsened process-induced variation, and statistical measurement is essential to monitor and control the variability. The benchmark circuit design and test should be scalable in time, reliability, and design complexity. Digital system performance and variability have been assessed with benchmark ring oscillators (ROs), and it has been shown that well-designed ROs are useful to provide reasonable estimation accuracy in microprocessor performance [3], [4]. Especially, FEOL-only ROs are insufficient to predict BEOL-loaded real product performance. Therefore, in-situ and at-speed characterization of FEOL device and nBEOL interconnect with scalable and statistical testability becomes essential for reliable microprocessor performance gauge circuit.

II. Logic Interconnect Device

This paper proposes a logic interconnect device (LID) to characterize nBEOL parasitics, whose concept diagram is in Fig. 1. The LID utilizes a product inverter-based logic as a reference, and nBEOL wires are added with design intentions

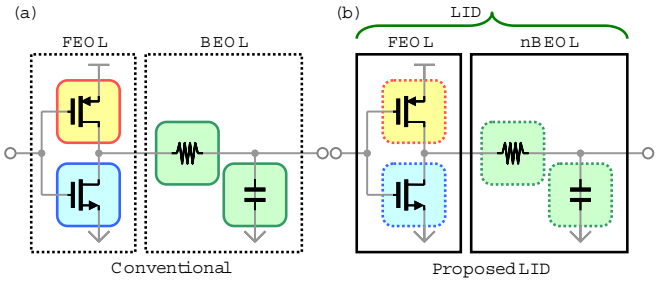

Fig. 1. (a) Conventional divide-and-conquer discrete FEOL and BEOL characterization. (b) Proposed parasitic parameter estimation using logic interconnect device (LID). An LID consists of a reference product-based logic and a well-defined nBEOL wiring. It captures in-situ and at-speed nBEOL parameters, FEOL-to-BEOL interactions, and process artifacts.

to distinguish parasitic component effects in real-time and in situation. For example, the contact, M1, V1, and M2 have bigger impacts than upper layers, because they are closer to FEOL and used most frequently for local wiring. The resulting parameters are effective nBEOL resistance, capacitance, sheet resistance, and dielectric constant. They are interpreted as in-situ and at-speed parameters observed by the product logic circuits. Conventionally, FEOL and BEOL are separately developed and characterized. The practice becomes less relevant in advanced CMOS technologies, where several processing techniques introduce interdependency. The OPC introduces modifications so that nBEOL in the absence of FEOL would be different from nBEOL with FEOL. Also the FEOL and nBEOL interact through parasitics and FEOL enhancement techniques, so that a divide-and-conquer approach would overlook the coupling. The interactions necessitate the simultaneous characterization of FEOL and nBEOL in positions. Differences between the proposed and conventional methods are arranged at Table I. By combining FEOL and nBEOL, the LID captures effective parasitics experienced by the product logic circuits in product-assimilated environment.

For at-speed measurements, 51-stage LID ROs are used to amplify technology performance and variation. The RO test parameters are quiescent current I_Q, active current I_A, and

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TABLE I
FEOL AND NBEOL TECHNOLOGY BENCHMARK

	Current	Presented
Approach	Divide and conquer	FEOL + nBEOL
Structure	Separate circuits	LID=Logic+nBEOL
Measurement		
At-speed	RO, passive	LID=Logic+nBEOL
In-situ	RO, FET	LID=Logic+nBEOL
nBEOL	DC parameter, network analyzer	LID performance comparison
Modeling coverage		
OPC	Not considered	Captured in LID
FEOL-nBEOL interaction	Not considered	Captured in LID
Model	Separate models	Logic+nBEOL as LID
Parameters		
Inverter	R_{inv}, C_{inv}	R_{inv}, C_{inv}
nBEOL	R_{BEOL}, C_{BEOL}	R_{LID}, C_{LID}

oscillation frequency f_O. Different nBEOL loads are added to the reference LID stage. Then the LID loading resistance ΔR_L and capacitance ΔC_L are calculated. There are several extraction algorithms as discussed in Section III. The employed LID nBEOL shapes and FEOL inverter diagrams are provided in Fig. 2. The shapes involve distributed line resistance and capacitance, and they are plugged into the LID nBEOL stage interchangeably.

There are 11 LID configurations in 65nm SOI CMOS as arranged in Table II. The unit inverter has two-finger NFET W_N=1.2μm and PFET W_P=1.8μm, and all 11 LIDs use the same unit inverter. The LID_0 serves as a reference LID without device-under test (DUT) nBEOL, and the LID FEOL inverter is defined as a rectangular area, including immediate nBEOL connections to the signal layer, as shown in Fig. 2(d). They are placed right next to another, so that the FEOL inverter effects can be de-embedded using DUT concept in other LIDs. For experiment, signal is limited in M2 layer, and M1 and M3 are used as isolation. The RO I_A, I_Q, and f_O are measured with in-line testers on the manufacturing floor during the wafer processing. The complete circuit can be tested at M4 or above.

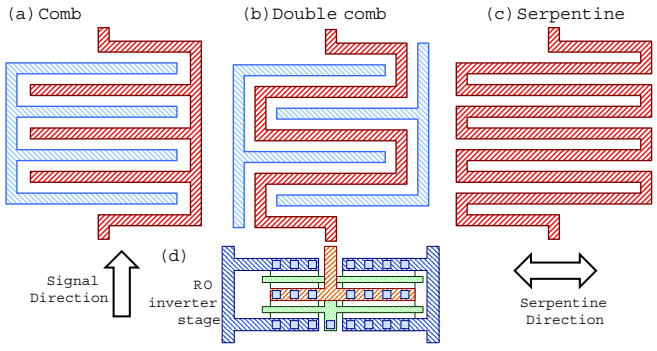

Fig. 2. LID nBEOL loading configuration diagrams. (a) Comb, (b) double comb, and (c) serpentine metal shapes are used in the LID. Light-colored shapes are connected to ground. (d) A unit LID inverter stage diagram.

TABLE II
LID CHAIN CONFIGURATION

LID #	M1 loading	M2 loading
0	none	none
1	comb	serpentine (L)
2	comb (1.5× wire width)	serpentine (L)
3	comb (2× wire width)	serpentine (L)
4	double comb	serpentine (L)
5	double comb (1.5× wire width)	serpentine (L)
6	double comb (2× wire width)	serpentine (L)
7	serpentine	serpentine (L)
8	serpentine (2× wire width)	serpentine (L)
9	serpentine	none
10	none	serpentine (W)

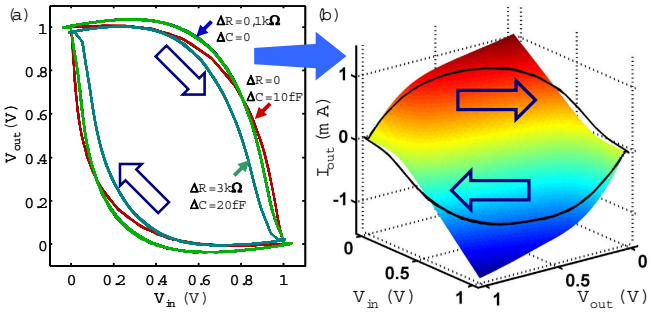

Fig. 3. An LID RO transient behavior. (a) The combinations of ΔR_L and ΔC_L generate nonlinear input and output traces for the LID. (b) The inverter current mapped along the inverter input and output trace. The ΔR_L and ΔC_L determine the trace, I_A, and f_O.

III. RO PARASITIC EXTRACTION

A. Unit Inverter and RO Analysis

The LID RO's f_O and I_A are determined by the loading resistance and capacitance. The interpretation of the in-situ LID RO behaviors becomes a separate challenge as plotted in Fig. 3. The model complexity and nonlinearity make it difficult to solve RO and LID analytically [5]. The RO's performance has been abstracted with I_A, I_Q, and f_O measurements. The I_A is converted as effective resistance $R_{eff} = V_{DD}/(I_A - I_Q)$. The capacitive load is obtained from the f_O as effective capacitance $C_{eff} = (N \times R_{eff} \times f_O)^{-1}$ [3].

B. DC nBEOL parasitic extraction

In the conventional divide-and-conquer approach, there are separate BEOL resistance and capacitance structures. The measured parameters are provided in the layout-to-netlist extraction tool. Using the LID layout and the extraction, the LIDs in Fig. 2 are converted to ΔR_{DC} and ΔC_{DC}. It is a common practice for layout-based simulation and model-to-hardware correlation (MHC), and it is not useful to explain the MHC discrepancy from processing disturbance and process-induced variations. It is compared with other estimation methods later.

C. Linearized nBEOL parasitic extraction

There is a reference LID_0 without nBEOL. One of the simplest methods is to subtract the obtained quasi-AC parasitic

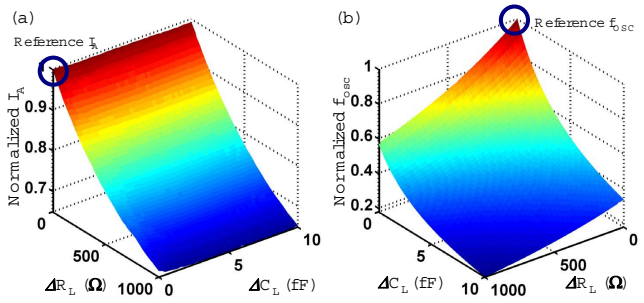

Fig. 4. (a) LID RO I_A and (b) f_O as a function of ΔR_L and ΔC_L. The RO shows highly nonlinear behavior with large ΔR_L and ΔC_L. When their ranges are near the reference, the slope becomes linear.

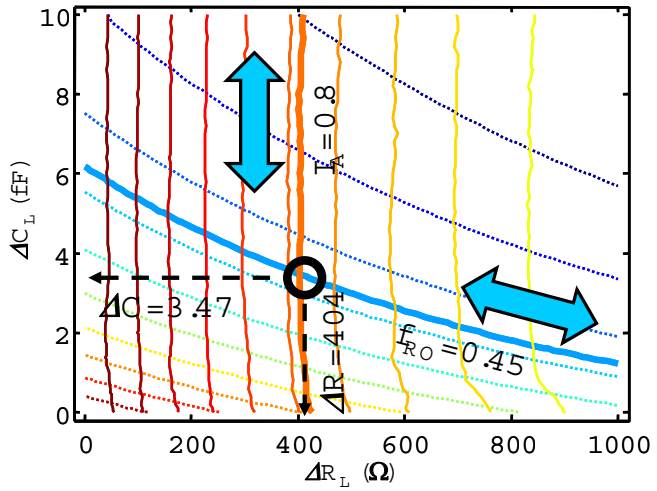

Fig. 5. Contour plots of LID RO equi-I_A and f_O levels. There are 2 unknowns - parasitic ΔR_L and ΔC_L. Using the measurement and the simulated equi-frequency and active current curves, the approximate $\Delta R_{L,mod}$ and $\Delta C_{L,mod}$ values are solved.

components from the reference [3]. The parasitic component differences are $\Delta R_{eff,k}$=$R_{eff,k}$-$R_{eff,0}$ and $\Delta C_{eff,k}$=$C_{eff,k}$-$C_{eff,0}$. By subtracting the reference, only nBEOL components are accounted for. The error will be larger at extreme values. It estimates parasitics well when the linearization is justified in given range, and a calibration process is involved.

D. Model-based nBEOL parasitic extraction

The LID behavior is highly nonlinear, and it is necessary to justify the linear approximation (III-C) in certain ranges with simulation, as shown in Fig. 4. The LID RO f_O is a nonlinear function of ΔR_L and ΔC_L, but the linear approximation is acceptable when the range is limited, e.g. near the reference. The plot enables model-based nBEOL parasitic estimation by finding out the intersecting $\Delta R_{L,mod}$ and $\Delta C_{L,mod}$ values using I_A and f_O, as plotted in Fig. 5. The contour lines of equi-I_A and f_O levels are obtained from Fig. 4. The solid lines are equi-current I_A levels, and the dotted lines are equi-frequency f_O levels. Ideally, the method provides highly accurate solutions. It relies on the accuracy of the FEOL+nBEOL MHC and transient simulation [4], [6].

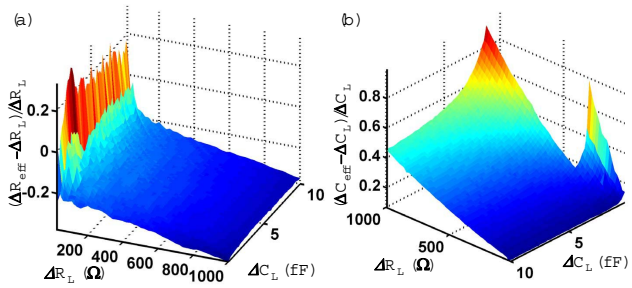

Fig. 6. The errors in parasitic extraction methods. (a) The relative error between the linearized resistance ΔR_{eff} and model-based ΔR_L is within ±30%. (b) The linearized capacitance ΔC_{eff} diverges against the loaded capacitance ΔC_L at small ΔC_L and large ΔR_L conditions.

When a technology matures with MHC, the model-based extraction becomes accurate, as it resolves FEOL nonlinearity precisely. The linearized parasitic nBEOL extraction (III-B) errors against the model-based nBEOL parasitic extraction are compared in Fig. 6. The plots show that ΔR_{eff} is within 30% of the ΔR_L, and the ΔC_{eff} extraction is close to ΔC_L at small ΔR_L, but it diverges at low ΔC_L region.

IV. nBEOL Parameter Estimation

A linear fitting and estimation tool is used to convert the LID RO measurements into nBEOL parameters so that conventional design automation tools can use them. By arranging M1 and M2 design parameters contributing to parasitic components, we have a set of linear equations for ΔR_{eff} and ΔC_{eff} in (1). The L/W refers to the length to width ratio of a metal wire, and A_X/d_X is area-distance ratio of a plate, between M1-to-M1, M1-to-M2, and M1-to-substrate. The α represents potential crosstalk between R and C components. The ΔR_{eff}, ΔC_{eff}, and all layout-dependent parameters are stacked as row vectors. We assumed the parameters have zero-mean. Thus, $[\Delta R_{eff} \quad \Delta C_{eff}]^T$ is a 2-by-10 matrix. Least-squares solution for this over-determined system is given as (2). The $X^\dagger$ is a pseudo-inverse of X, viz. $(X^TX)^{-1}X$. The nBEOL technology parameters, such as sheet resistance and dielectric constants are characterized in the fitting. The ΔR_{eff} and ΔC_{eff} are calculated from LID RO measurement. Also they are used to estimate $\Delta R_{eff,est}$ and $\Delta C_{eff,est}$ with the proposed equations. They are compared with ΔR_{DC} and ΔC_{DC} extraction (III-B) based on technology DC data, as plotted in Fig. 7. The $\text{LID}_{1,3,\cdots,9}$, and five other $\text{LID}_{2,4,\cdots,10}$ are independently used for fitting and testing. The DC-calculated ΔC_{DC} are close to the measurement and estimation. But the resistances ΔR_{DC} deviate significantly from the measurement. It implies that the DC parameters in technology data do not reflect realistic in-situ nBEOL parameters. The estimation errors for $R_{eff,est}$ and $C_{eff,est}$ are significantly less than the errors for DC calculation as arranged in Table III. Using the linearized parasitic extraction and the nBEOL parameter estimation, the nBEOL parameter process-induced variation is monitored in Fig. 8. The sheet resistance ρ and the dielectric constant ϵ are calculated with (1) and (2). The plots show

$$\begin{bmatrix} \Delta R_{eff} \\ \Delta C_{eff} \end{bmatrix} = \begin{bmatrix} \rho & \alpha_1 & \alpha_2 & \alpha_3 \\ \alpha_4 & \epsilon_0\epsilon_{M1,M1} & \epsilon_0\epsilon_{M1,M2} & \epsilon_0\epsilon_{M1,sub} \end{bmatrix} \cdot \begin{bmatrix} L/W \\ A_{M1,M1}/d_{M1,M1} \\ A_{M1,M2}/d_{M1,M2} \\ A_{M1,sub}/d_{M1,sub} \end{bmatrix} + \begin{bmatrix} b_R \\ b_C \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \rho & \alpha_1 & \alpha_2 & \alpha_3 \\ \alpha_4 & \epsilon_0\epsilon_{M1,M1} & \epsilon_0\epsilon_{M1,M2} & \epsilon_0\epsilon_{M1,sub} \end{bmatrix} = \begin{bmatrix} L/W \\ A_{M1,M1}/d_{M1,M1} \\ A_{M1,M2}/d_{M1,M2} \\ A_{M1,sub}/d_{M1,sub} \end{bmatrix} \cdot \begin{bmatrix} \Delta R_{eff} \\ \Delta C_{eff} \end{bmatrix}^{\dagger} \quad (2)$$

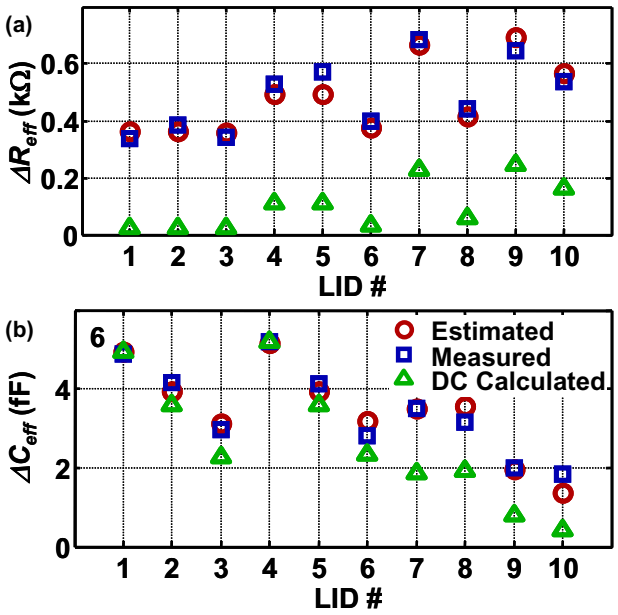

Fig. 7. The comparison of estimated, measured, and DC-calculated (a) ΔR_{eff} and (b) ΔC_{eff}. The parameters are obtained from layout, hardware measurements, and calculated at DC using current technology parameters. For linear fit estimation $\text{LID}_{1,3,\cdots,9}$ are used for fitting, and others ($\text{LID}_{2,4,\cdots,10}$) are exclusively used as a testing set.

TABLE III
nBEOL Parameter Discrepancy

	$\Delta R_{eff,est}$ error (%)		$\Delta C_{eff,est}$ error (%)	
	LID	DC	LID	DC
LID_2	-5.5%	-8.8%	-5.2%	-13.3%
LID_4	-6.5%	-17.2%	-0.7%	-1.1%
LID_6	-5.3%	-9.6%	12.9%	-16.7%
LID_8	-6.1%	-12.9%	13.0%	-38.8%
LID_{10}	-5.9%	-9.2%	-25.7%	-76.3%

that the proposed method effectively reveals the 65nm CMOS technology's nBEOL parameter process variation.

The resulting parameters provide better MHC for nBEOL loaded FEOL than conventional methods. The linear combination of the nBEOL LIDs leads to a more reliable digital system benchmark metric to evaluate microprocessor performance and yield before packaging.

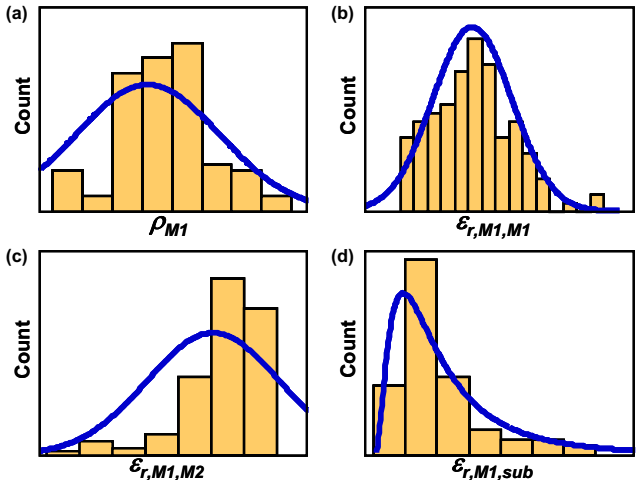

Fig. 8. Variation of (a) sheet resistance, and (b) - (d) dielectric constants. The sheet resistance, and dielectric constants are calculated by the proposed linearized parasitic extraction and linear fitting method, for available 135 chips. The relative frequency for each parameter is shown.

V. Conclusion

We presented a methodology to characterize BEOL interconnect parasitics considering front-to-back-end interaction in-situ and at-speed operating conditions. Using LIDs, technology parameters such as sheet resistance and dielectric constant were estimated more accurately than conventional DC-based and divider-and-conquer extraction tools.

VI. Acknowledgment

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