Early Prediction of Product Performance and Yield Via Technology Benchmark

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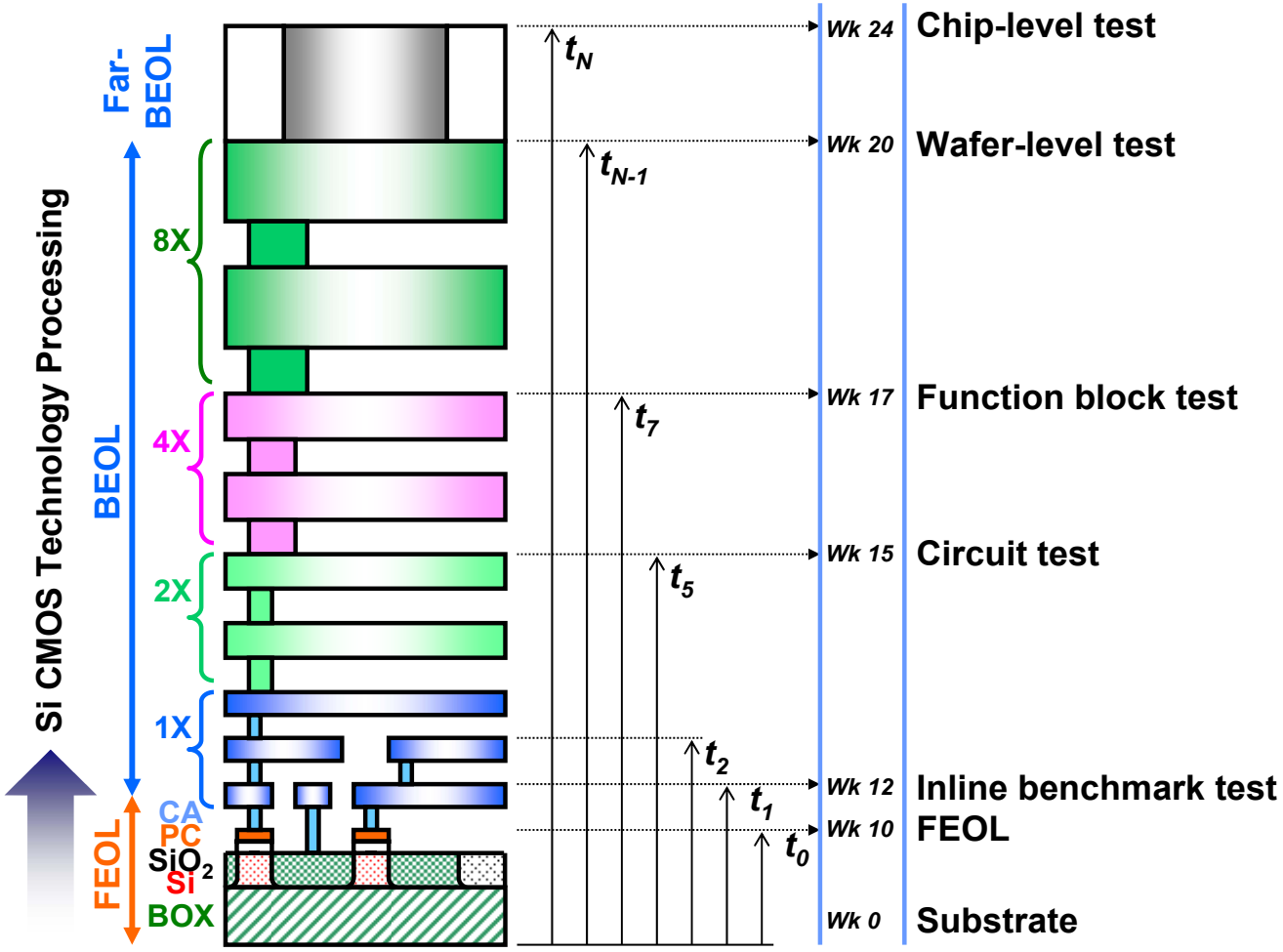
Background

- **Process variation as grave concern:**
  - **Limits IC product performance and yield**
  - **Difficult to model / predict before tape-out**

- **Product circuit is tested and qualified usually after BEOL process is complete**
  - **Test for final product is often expensive in terms of cost, time and resource**

Background

- **Typical schedule for CMOS technology development and testing:**

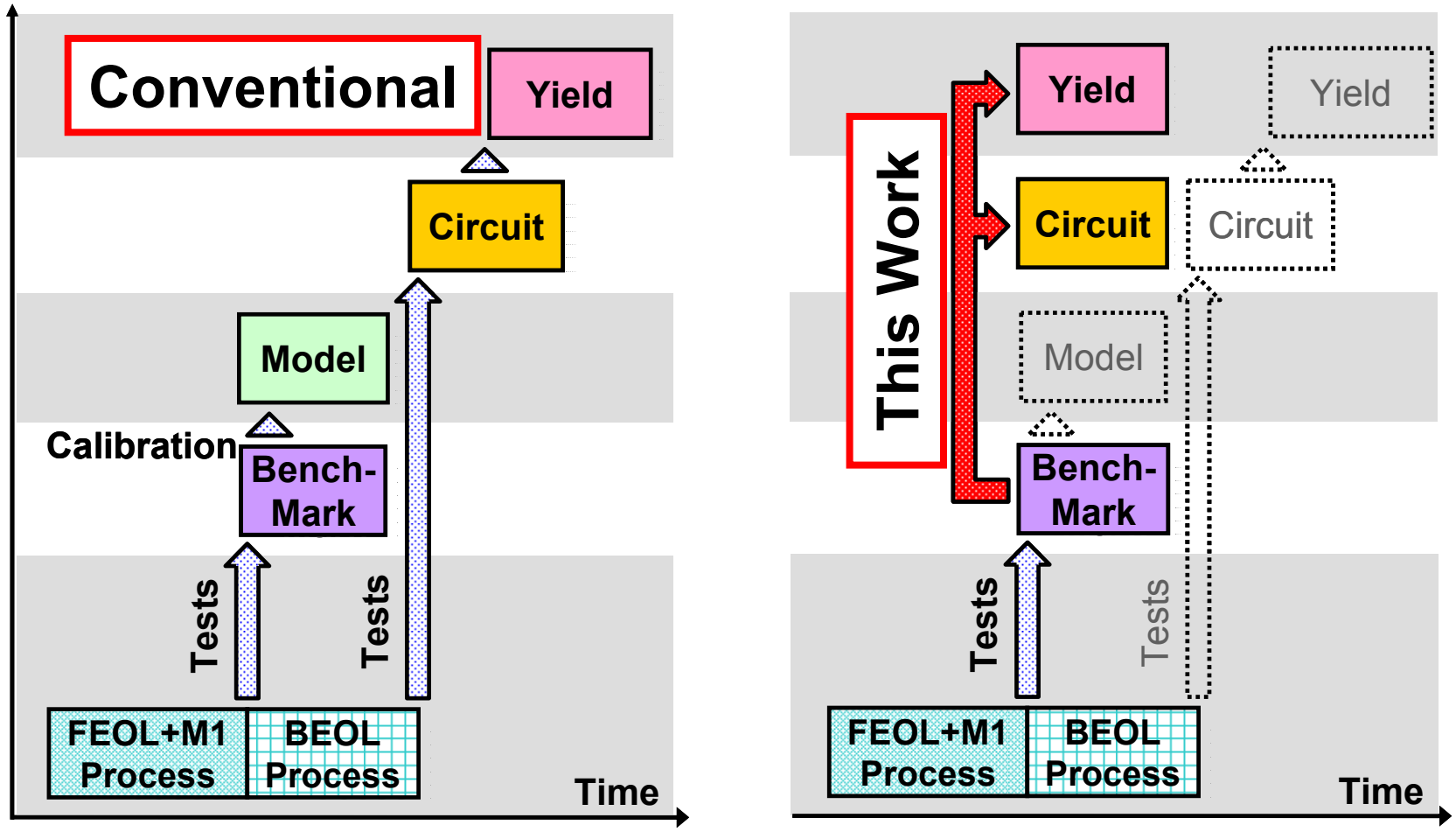


Step	Level	Time (Week)	Test
t_N	C4	24	Chip
t_{N-1}	M_{top}	20	Wafer
t_5	M_5	15	Block
t_1	M_1	12	Inline
t_0	FEOL	10	-

Motivation

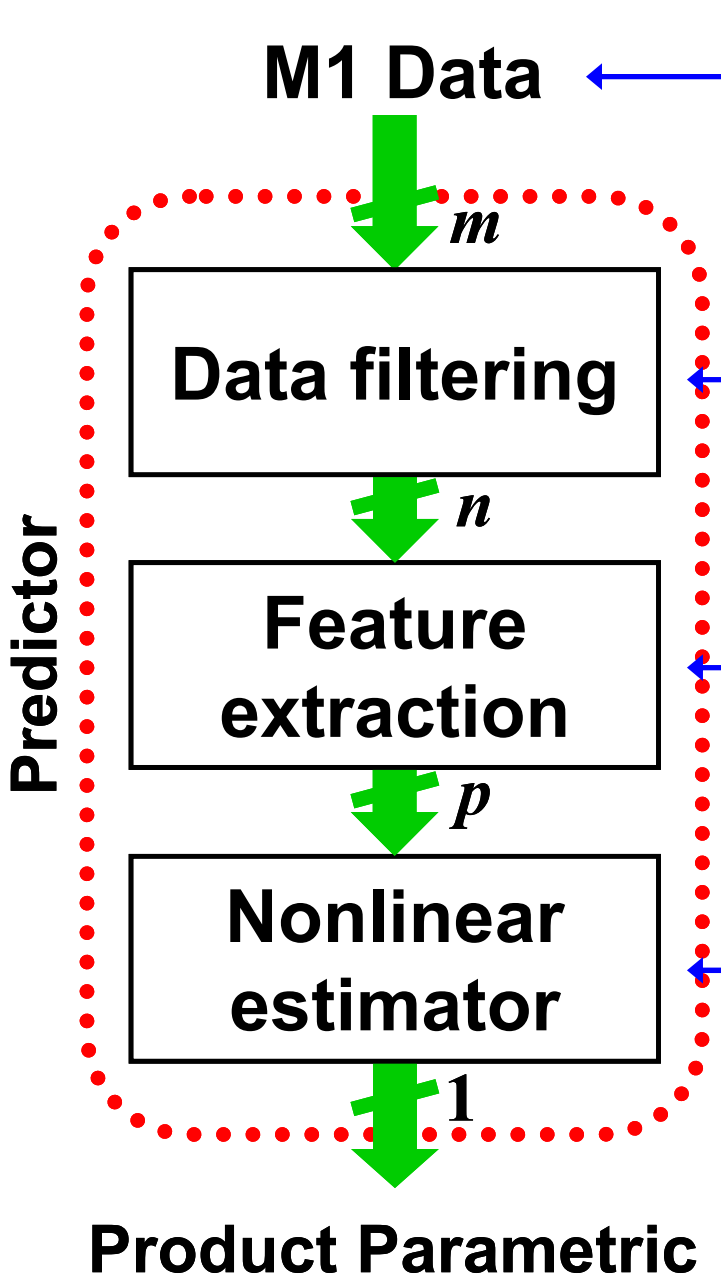
- **Use existing M1 data to predict product performance / yield**
  - **Device characterization is available early in manufacturing, typically at M1 level**
  - **M1 test data, if prudently selected, carries relevant information to reliably predict product performance and yield**

Motivation



- **Will reduce test cost and time for product circuit performance / yield**

Methodology



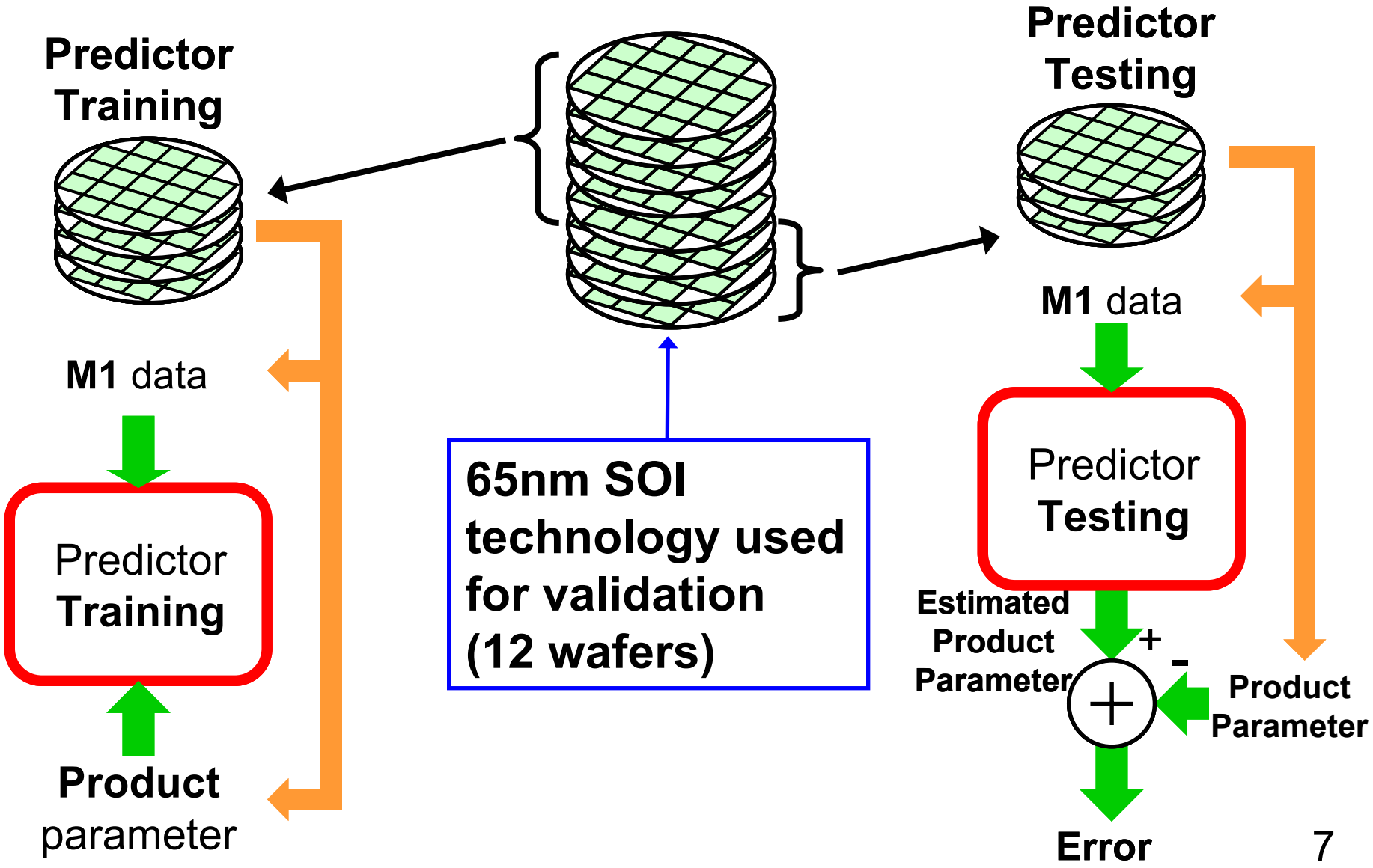
Well-chosen M1 data captures key process variation mechanisms (Vth, Tox, Lpoly, etc)

Remove outlier and statistically unimportant parameters

Use projected principal component to extract features while preserving most information relevant circuit parameters

Neural net is employed to estimate product performance or yield

Training and Testing



Experiment: 65nm SOI

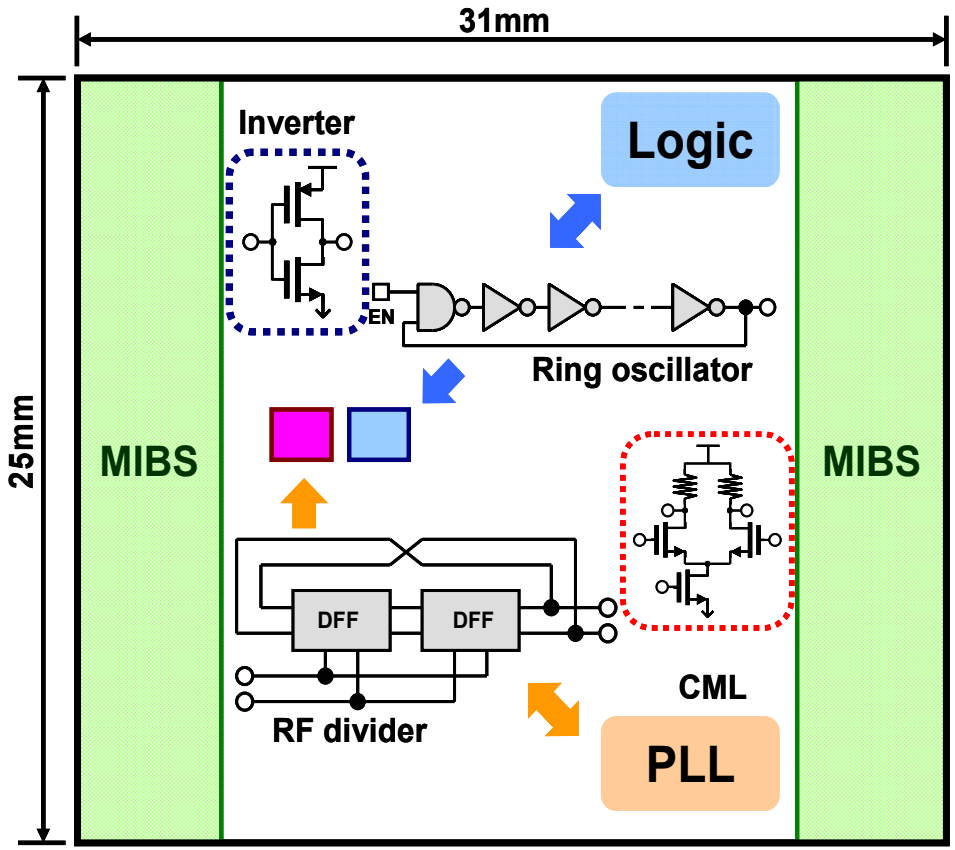
- **M1 data set as an input:**

M1 test structure category	# of parameters (before screening)	# of parameters (after screening)
FET	1,988	759
RO	248	83
SRAM	398	159
Capacitance	222	108
Total	2,856	1,109

- **10 wafers used for training, 2 wafers used for testing**

Validation Circuit

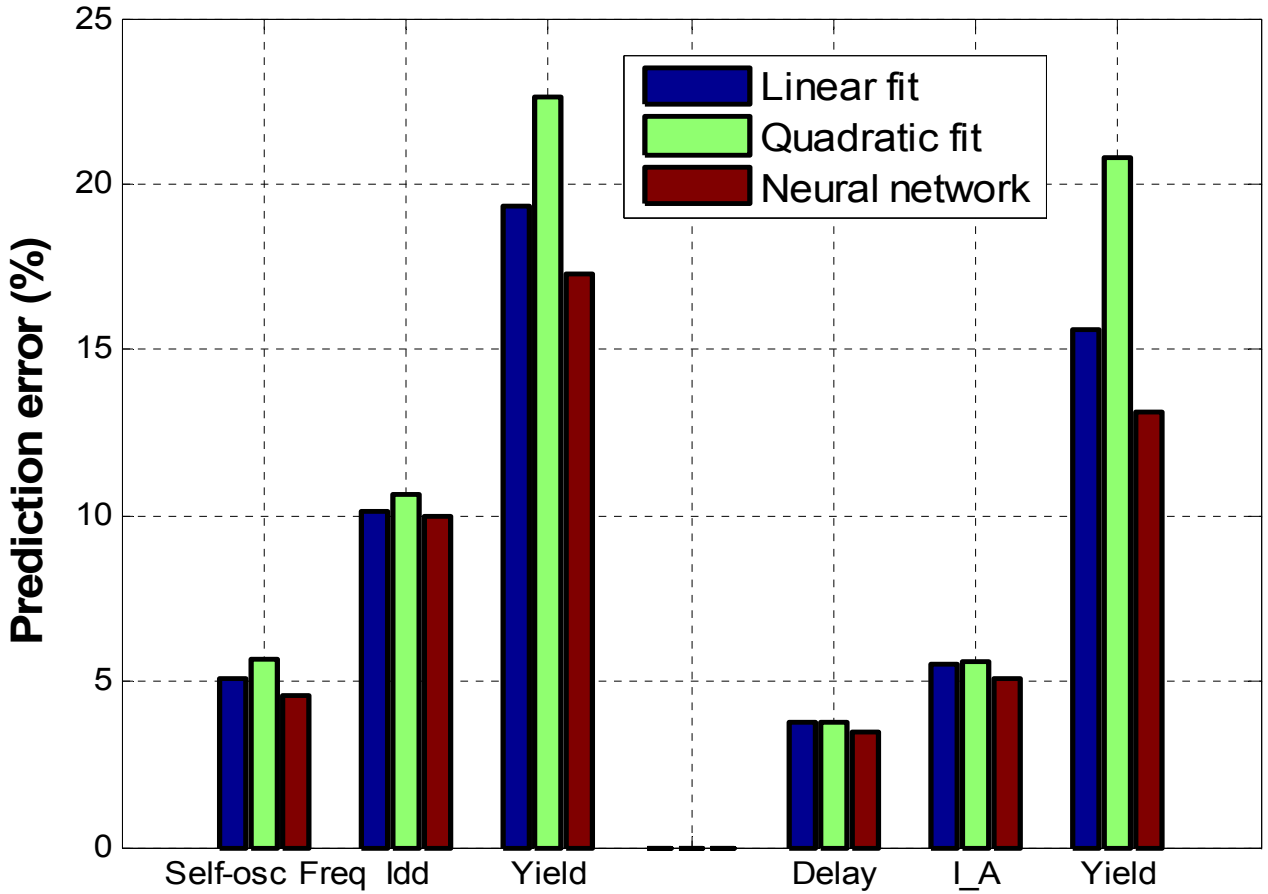
- Two product circuits chosen for validation of proposed method
  1. Freq. divider as PLL component: self-osc freq. is estimated
  2. Ring oscillator as logic product: gate delay of 101-stage inverter-based RO is predicted



Prediction Results

	Estimated parameter	Mean	Std dev	Neural Net %err
Freq divider	Self-osc freq.	34.6GHz	2.9GHz (8.3%)	4.6%
	Idd	24.0mA	3.6mA (15.1%)	10.0%
	Yield	27.5%	-	17.7%
Ring Osc	Delay	4.3ps	0.37ps (8.7%)	3.5%
	$I_{A,RO}$	2.5mA	0.28mA (11.1%)	5.1%
	Yield	25.6%	-	13.1%

Prediction Results



- **Neural net is slightly more accurate than linear estimator**
- **Error comes mainly from: (1) BEOL variation and (2) Intra-die variation**

Prediction Robustness

- To evaluate the estimation robustness, training and testing data sets are divided to slow and fast, and prediction was performed
- The prediction error does not strongly depend on any particular combination of training / testing data sets
- The proposed method is **robust even when wafer variation is significant**

Training set	Testing set	%err
Slow	Slow	4.5%
Slow	Fast	5.6%
Fast	Slow	5.5%
Fast	Fast	4.9%

Feedback to Design / Tech

- **Mapping from M1 measurement to product performance metric:**
  - **For technology, it reveals what device characteristics are most sensitive to product, and to what degree**
  - **Designer can make educated trade-off between design parameters**
  - **E.g. RO gate delay is related to tech parameters:**

$$\tau \propto I_{on} + 0.817 I_{off} + 0.765 V_{th}$$

(each parameter normalized)

Conclusion

- **Proposed an efficient statistical method to predict circuit performance and yield solely based on technology benchmark data available at M1**
  - **<5% error for estimating mmWave freq. divider performance**
  - **<4% error for RO gate delay**
- **This method significantly cuts time and cost of final product test**